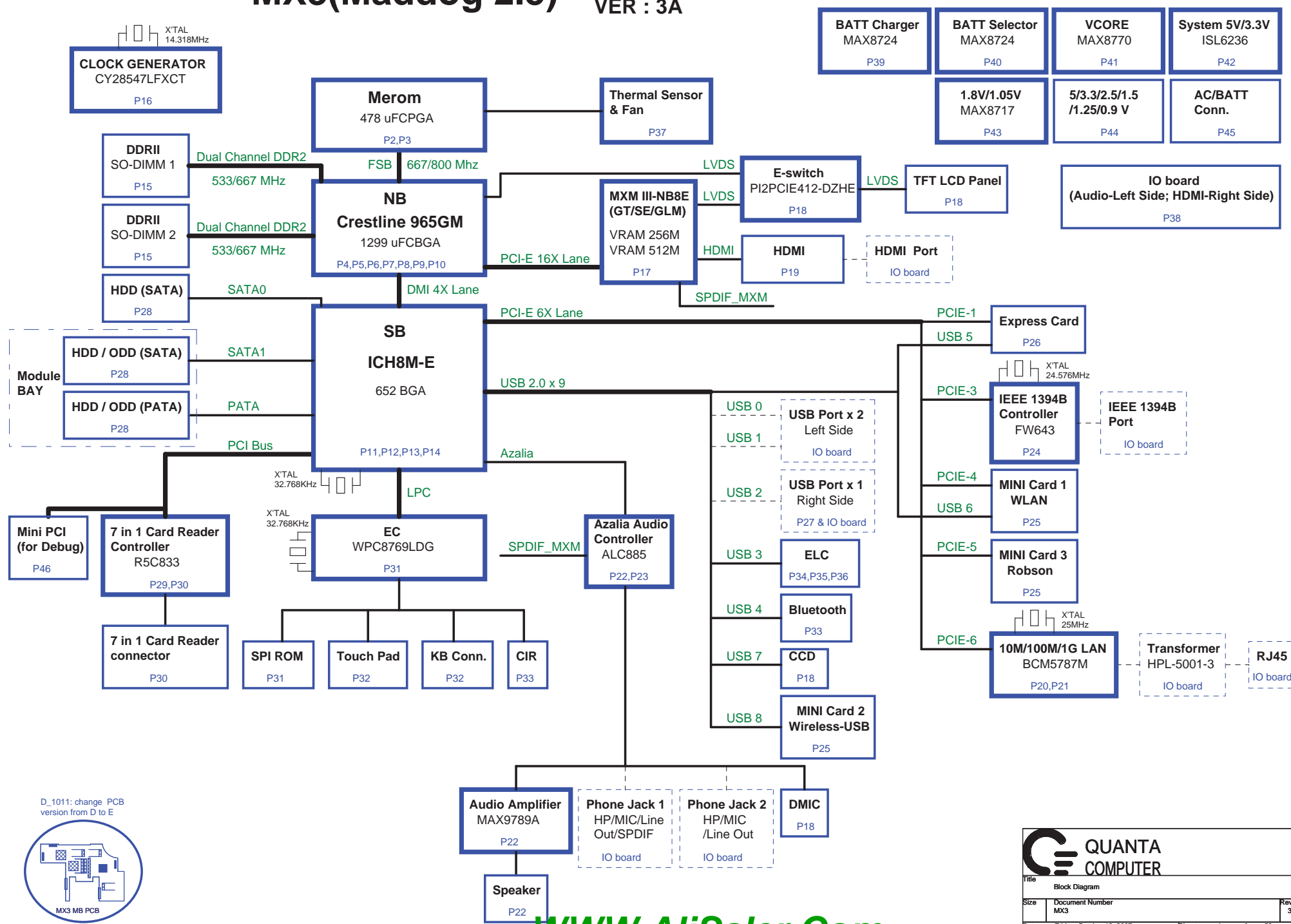
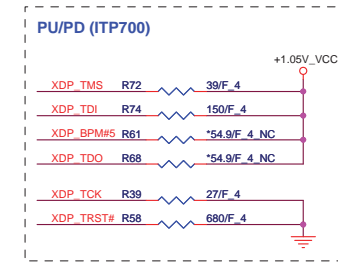
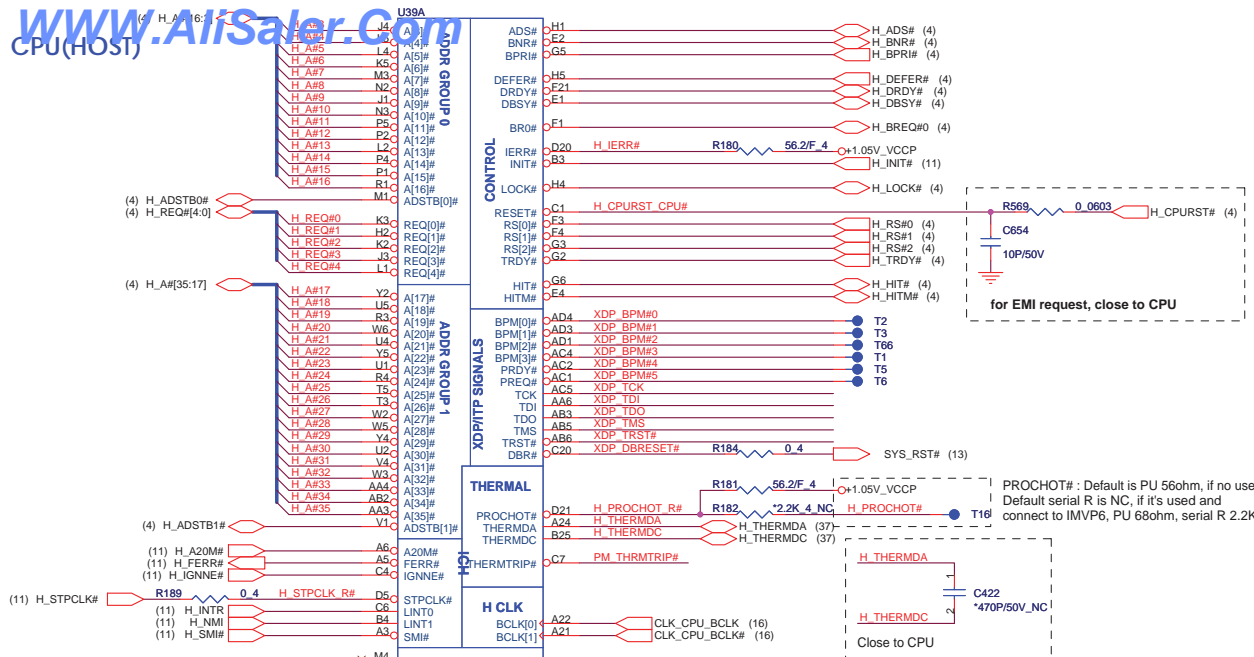
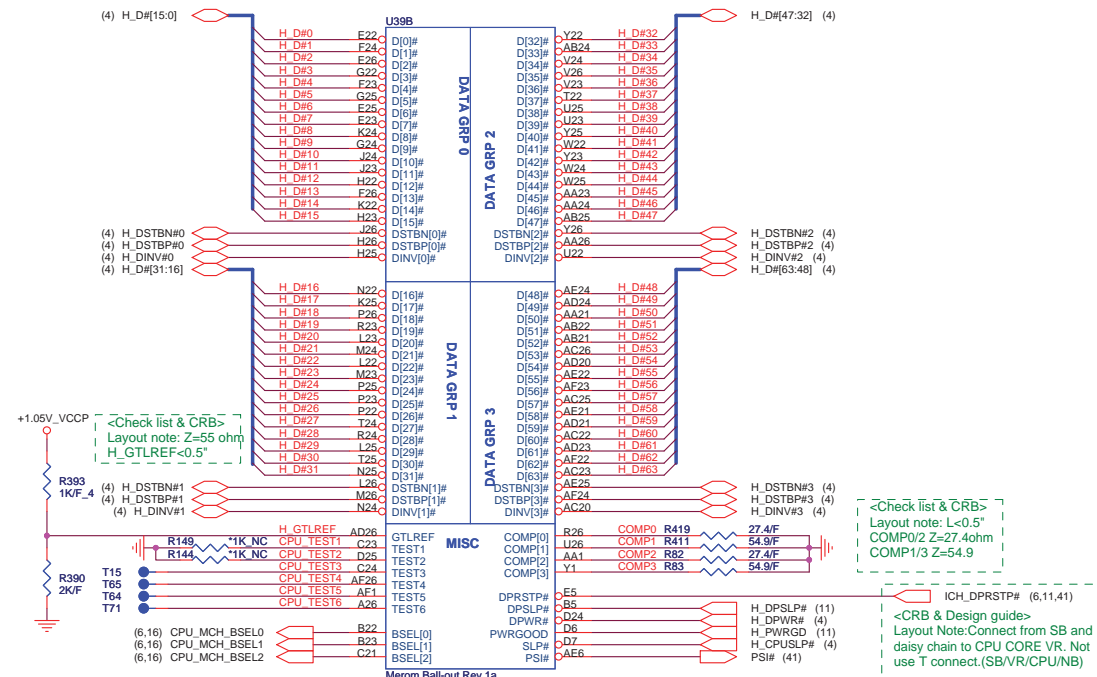
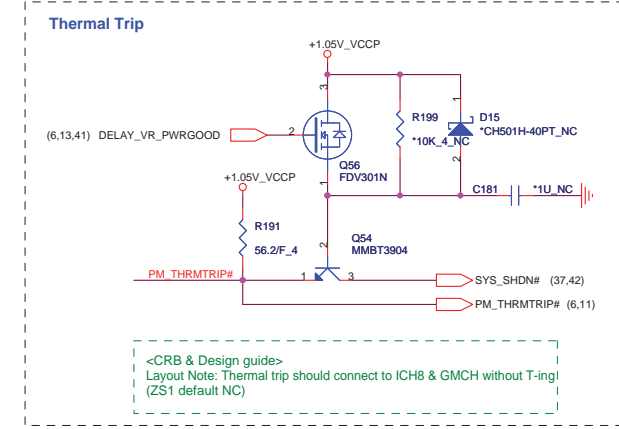


MX3(Maddog 2.5) VER : 3A




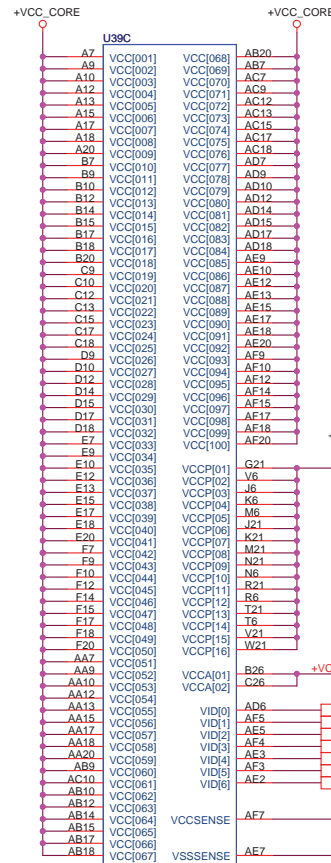
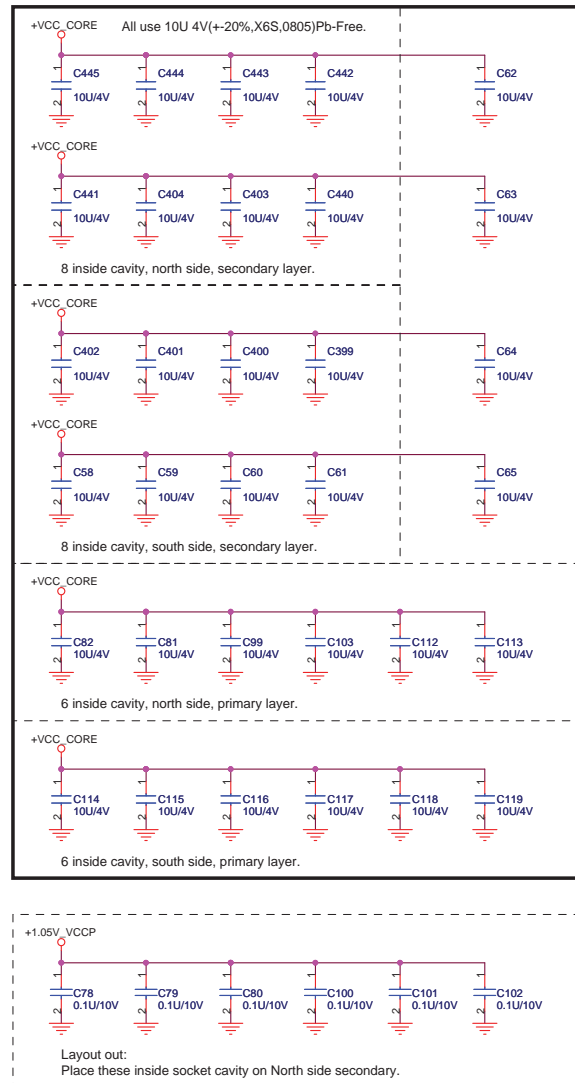


ITP disable guidelines			
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	PU Depop	+3.3V_RUN	Close to CK505 Pin37



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

 QUANTA COMPUTER			
Title CPU Host(1/2)			
Size	Document Number MX3		Rev 2A
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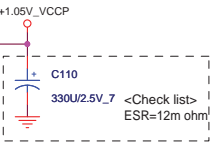


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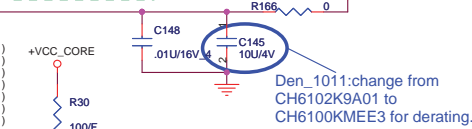
Ivcc Max 52A

Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)

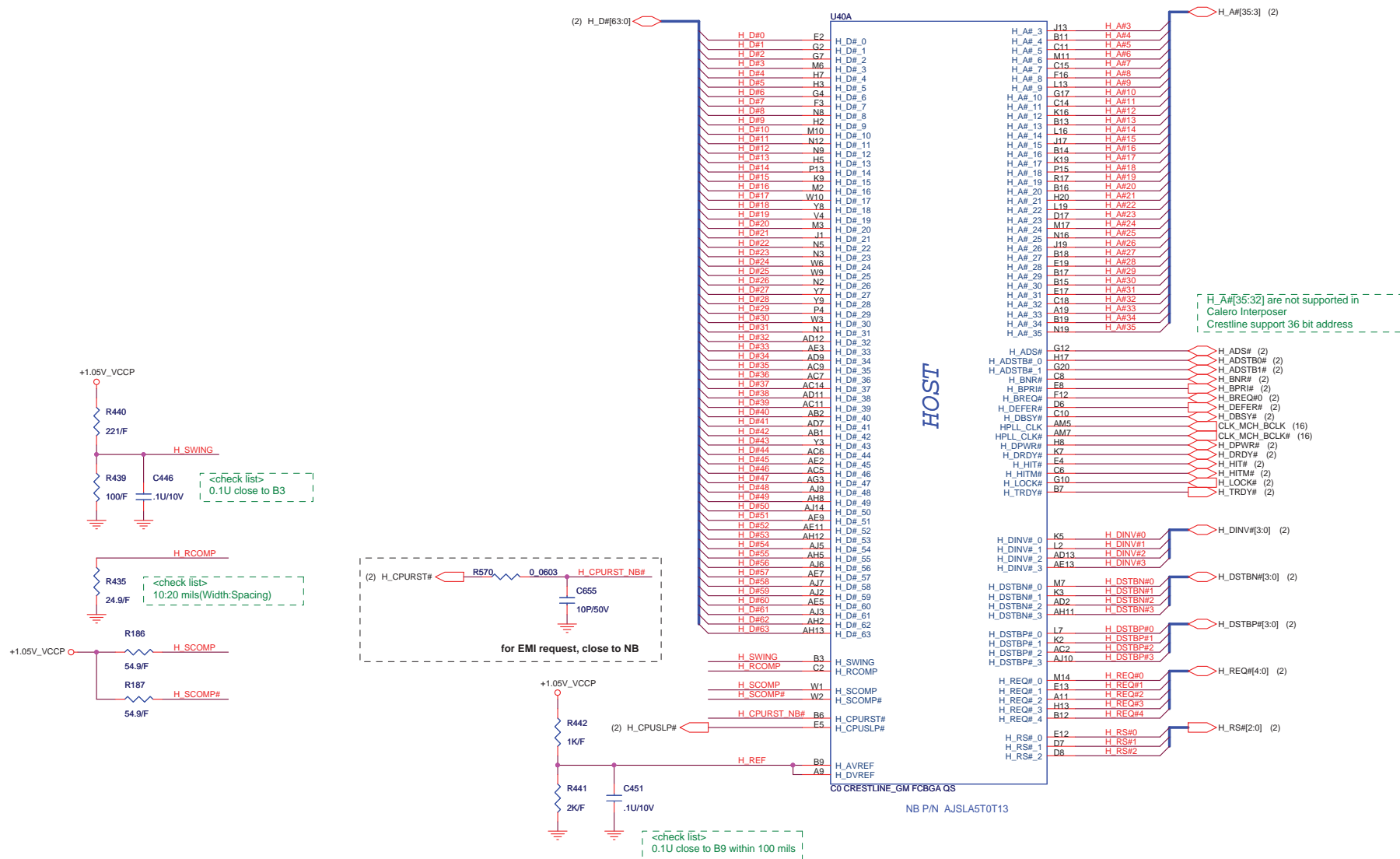
Ivcca Max 130mA

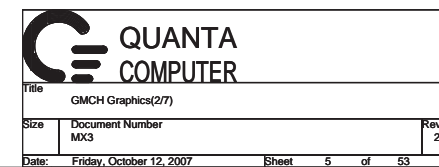


<CR6>
.01U near to B26 ball



<Demo board>
Routing 27.4ohm with 50mils spacing
PU/PD near to CPU 1"

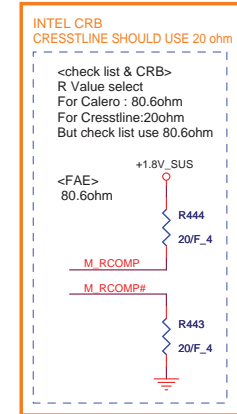
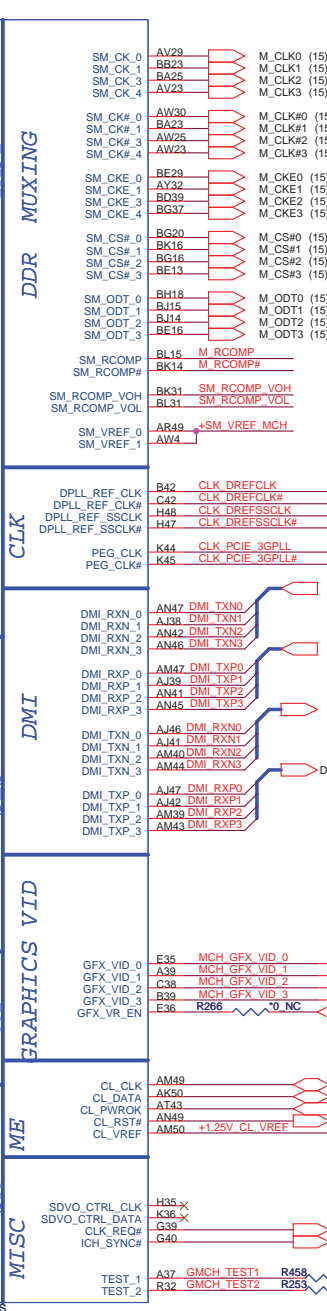
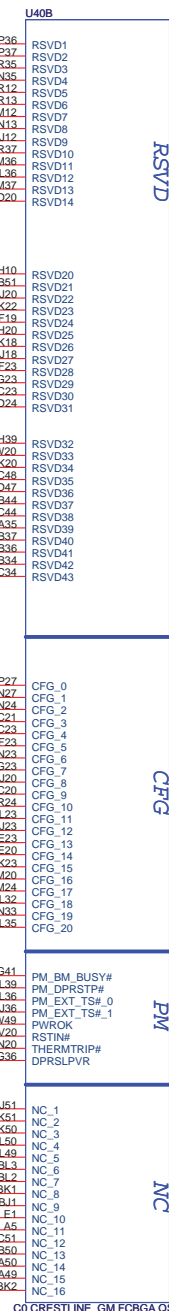
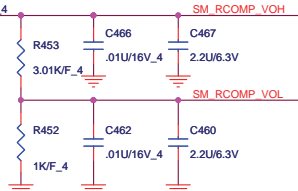
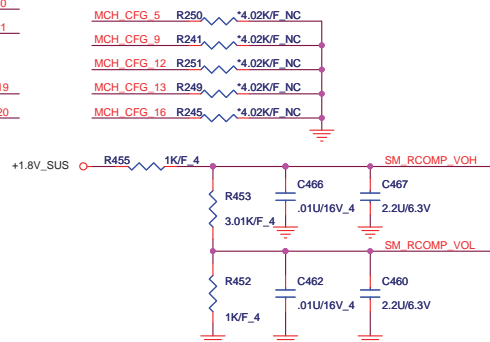
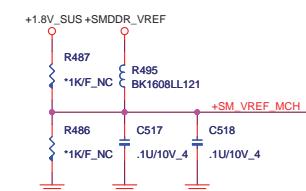
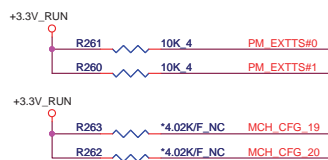
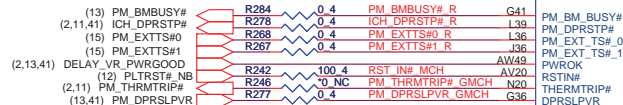
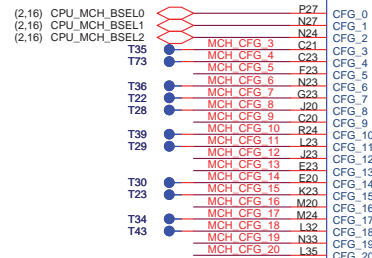




All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Reserved 01 = ALL-Z Mode Enabled 10 = XOR Mode Enabled 11 = Clock Gating Enabled (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIe x1 is operation (Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
ADD 0.1UF

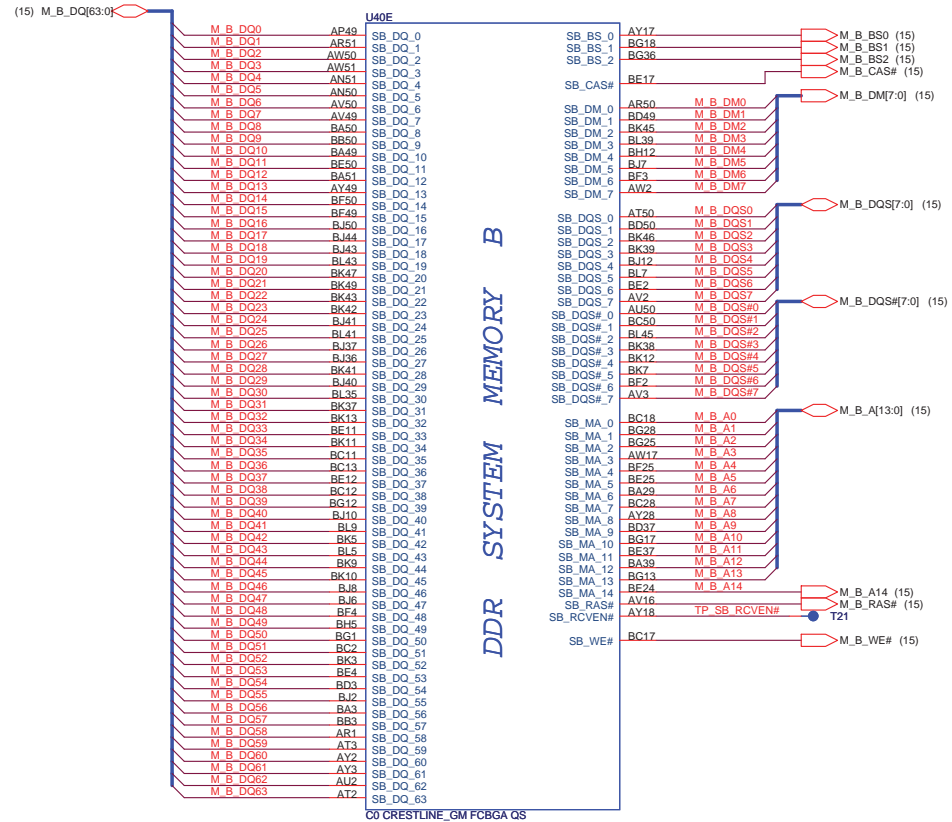
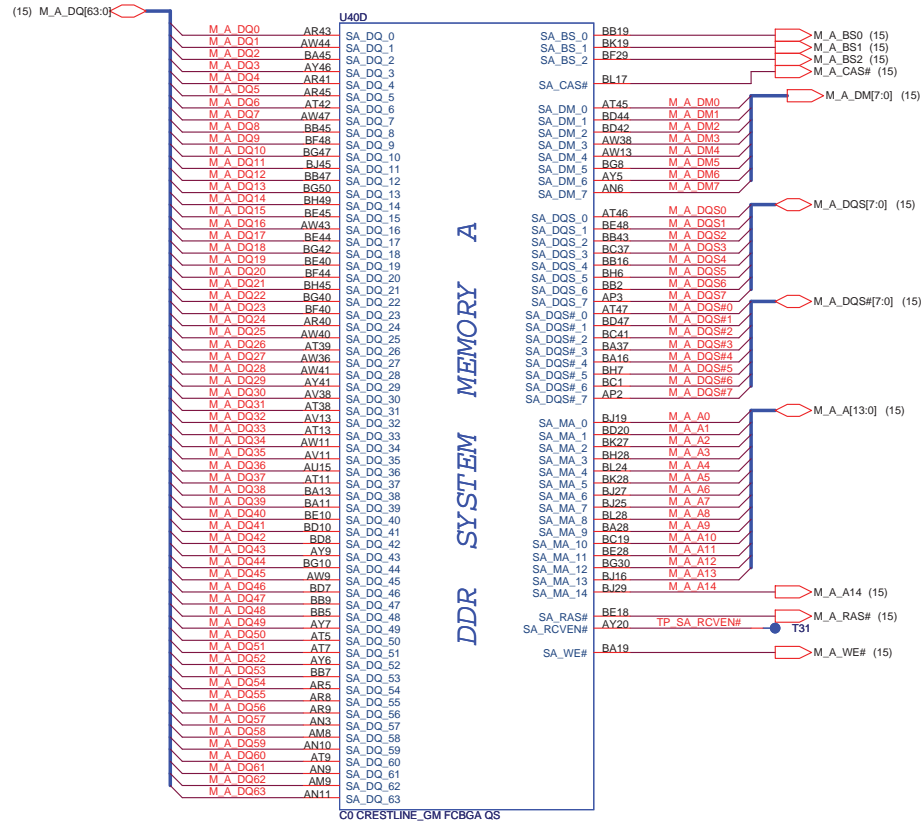


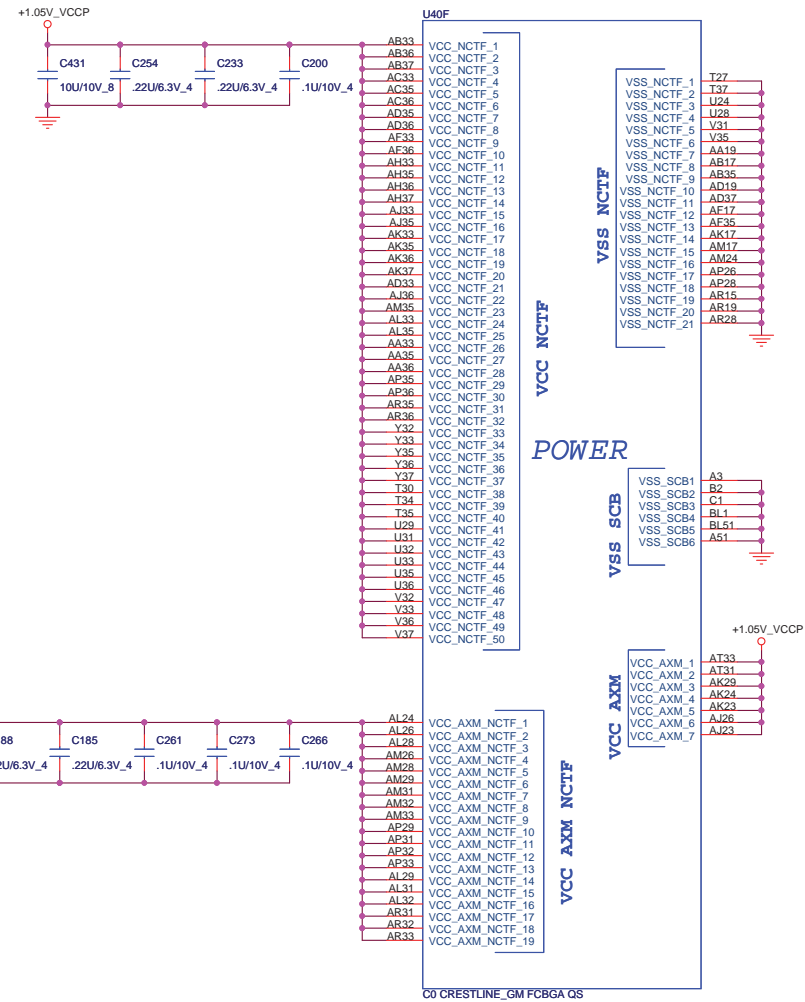
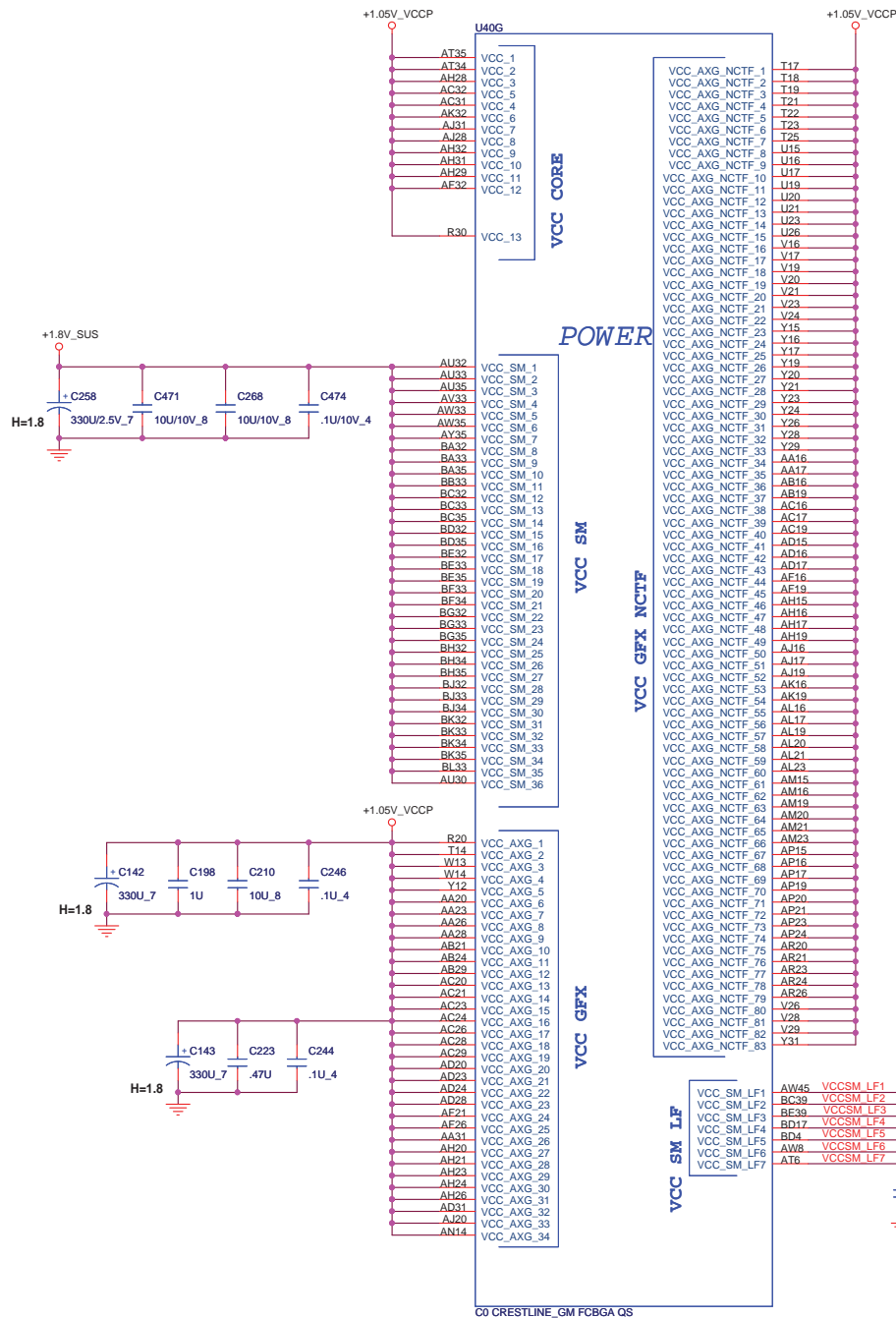
QUANTA COMPUTER

Title: GMCH Strapping(3/7)

Size: Document Number MX3 Rev 2B

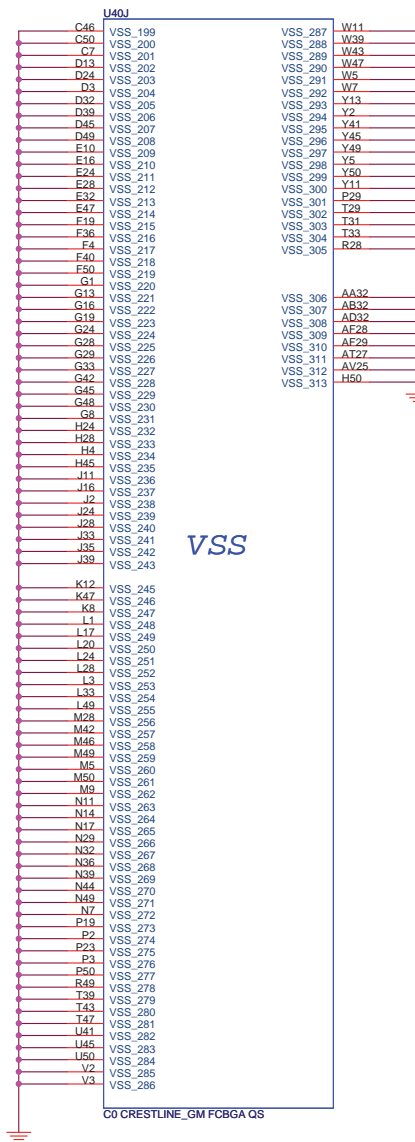
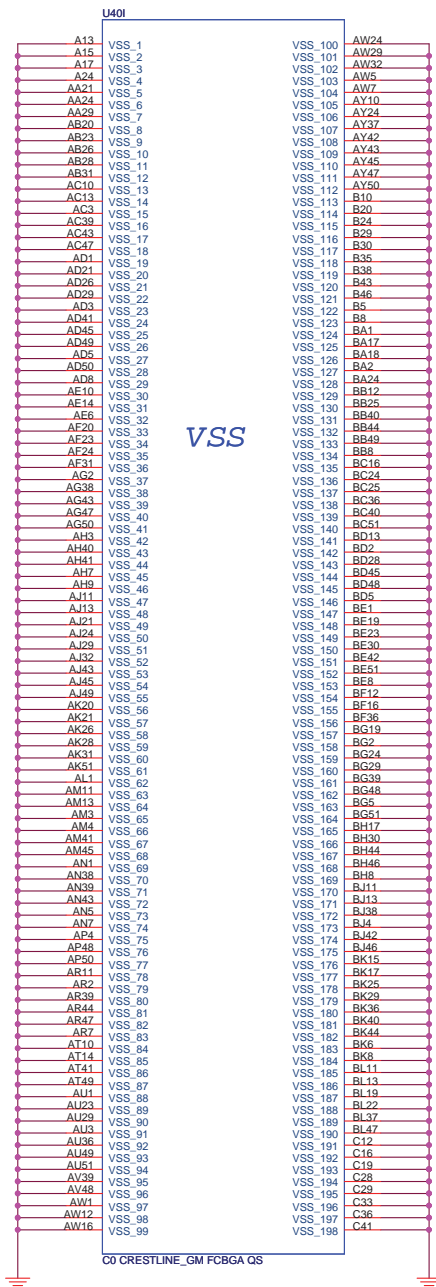
Date: Friday, October 12, 2007 Sheet 6 of 53






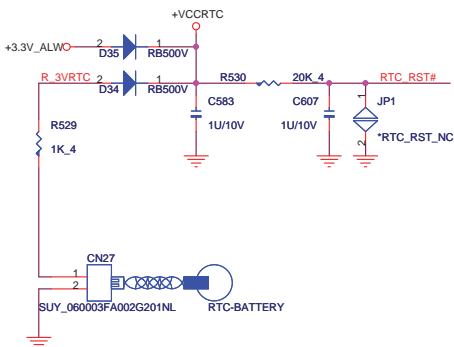
Title			
GMCH Power-1(5/7)			
Size	Document Number	Rev	
MX3		2B	
Date:	Friday, October 12, 2007	Sheet	8 of 53





 QUANTA COMPUTER	
Title GMCH Power-3(7/7)	
Size MX3	Document Number Rev 2B
Date Friday, October 12, 2007	Sheet 10 of 53

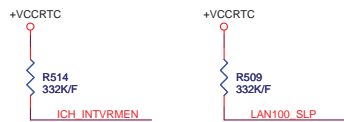
RTC



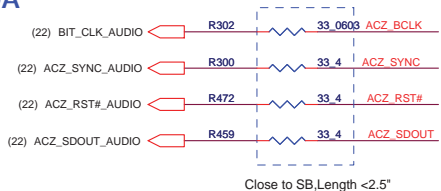
SB Strap

As Intel's review(Apr.,17,2007), internal VR must be enabled.

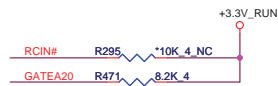
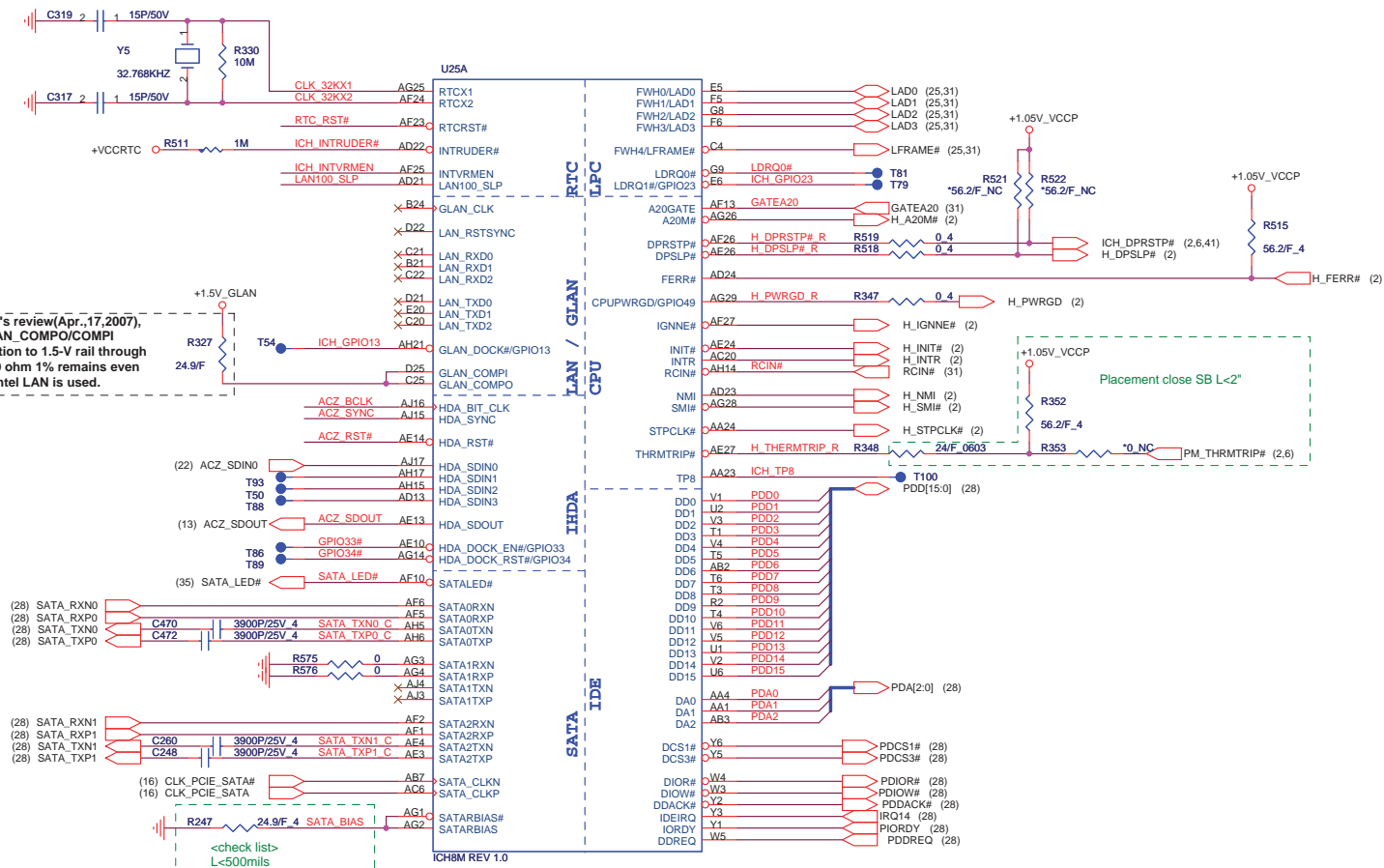
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



HDA



As Intel's review(Apr.,17,2007), the GLAN_COMPO/COMPI connection to 1.5V rail through the 24.9 ohm 1% remains even if non-Intel LAN is used.

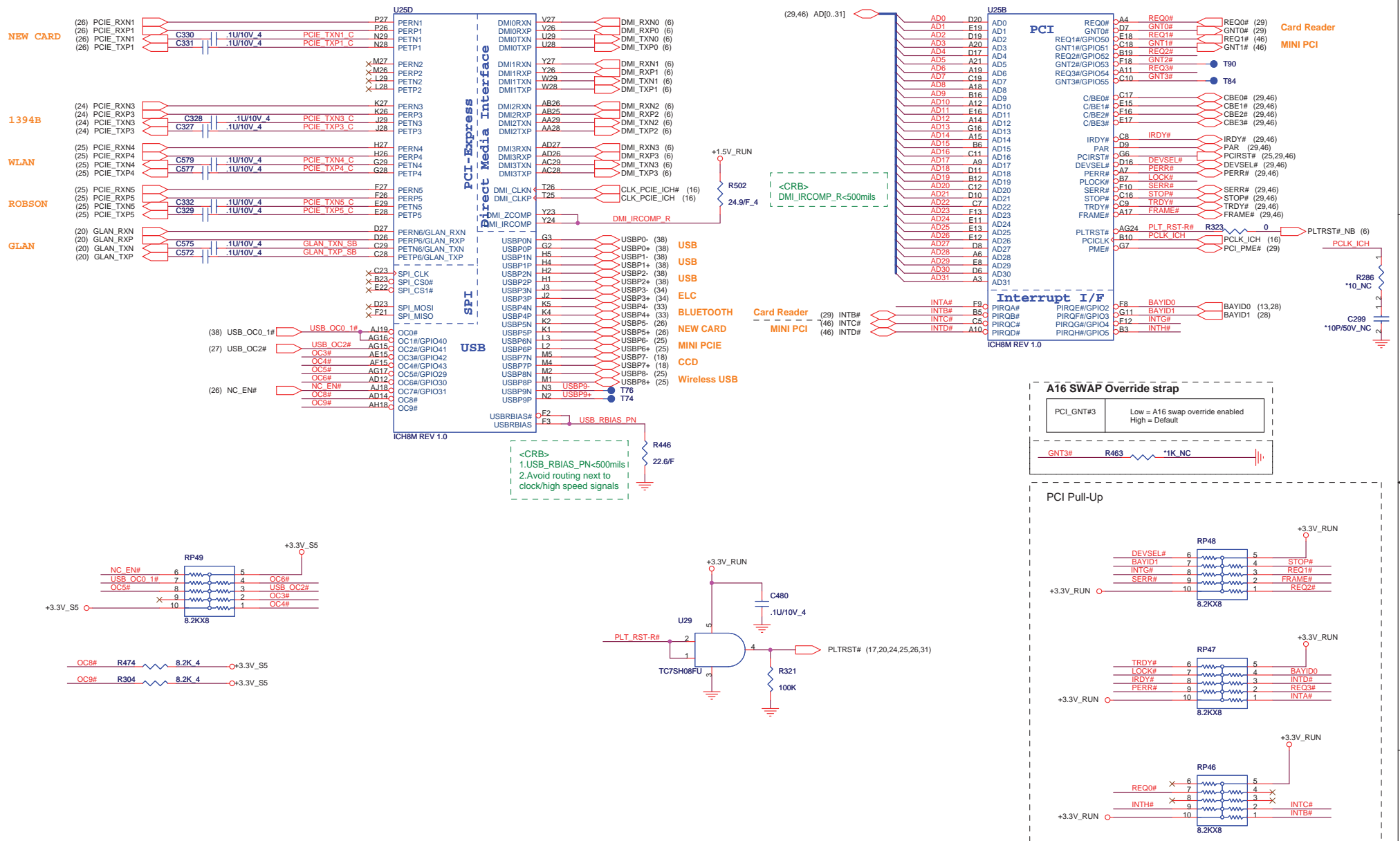


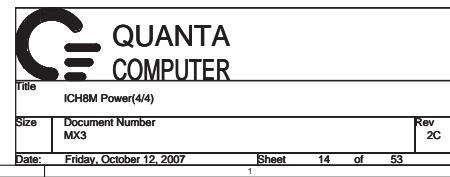
QUANTA COMPUTER

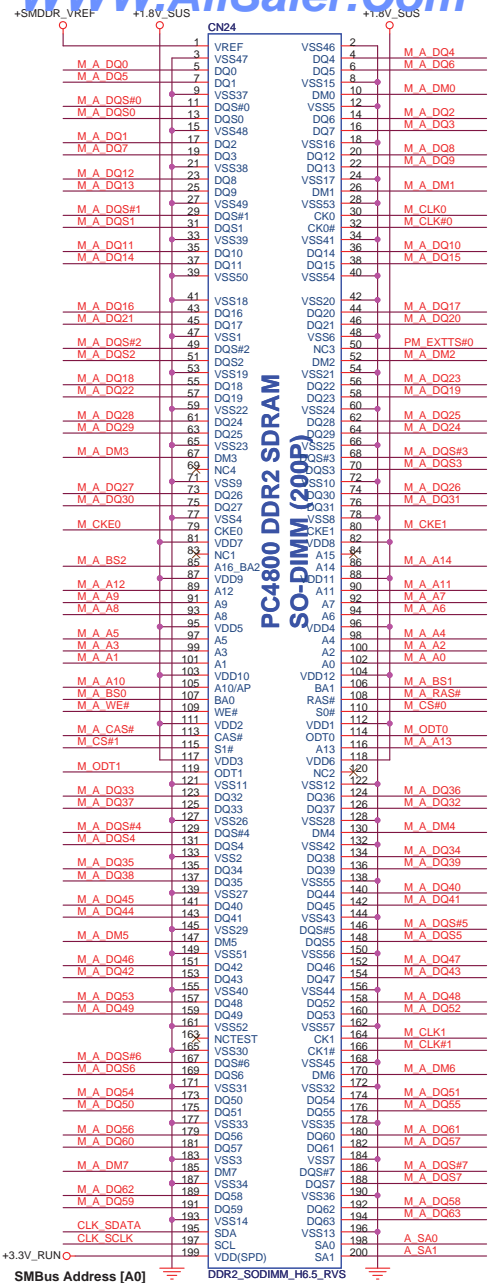
Title: ICH8M Host(1/4)

Size: Document Number MX3 Rev 2B

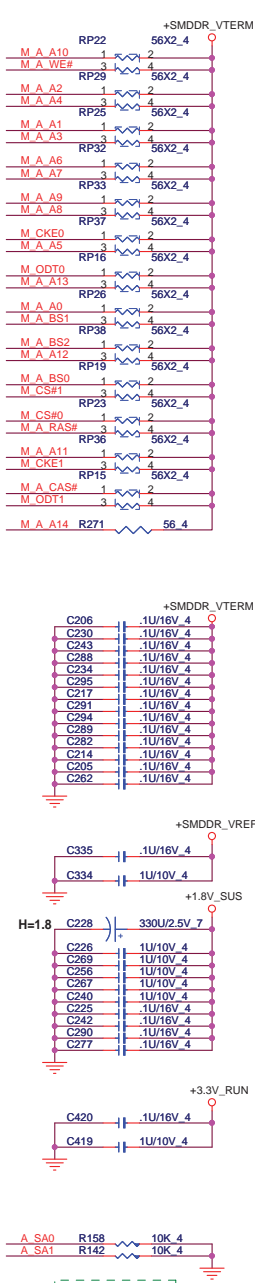
Date: Friday, October 12, 2007 Sheet 11 of 53

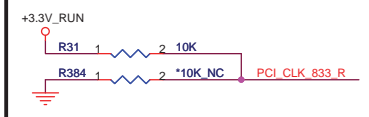






SO-DIMM0



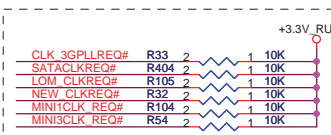
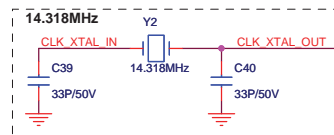


PCI_CLK_833_R = PCI2/TME, Internal PU 100K

PCI2/TME	PIN32
0	Normal mode
1(Default)	Trusted mode

PCLK_ICH_R = PCIF0/ITP_SEL, Internal PD 100K

PCIF0/ITP_SEL (PIN37)	PIN5	PIN6
0(Default)	SRCT_10	SRCC_10
1	CPUT2_ITP	CPUC2_ITP

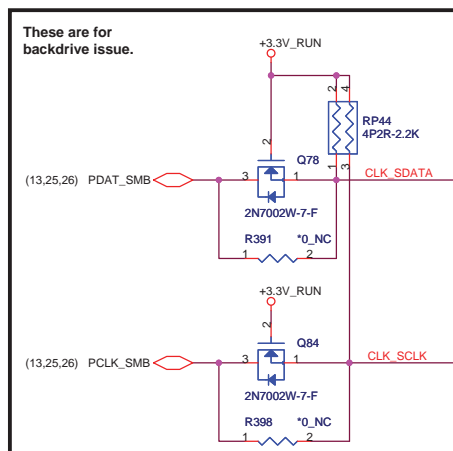
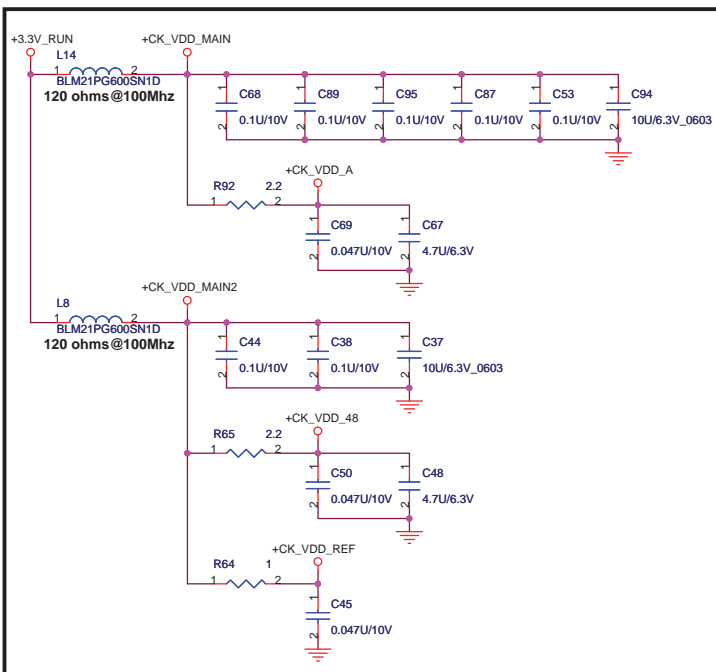
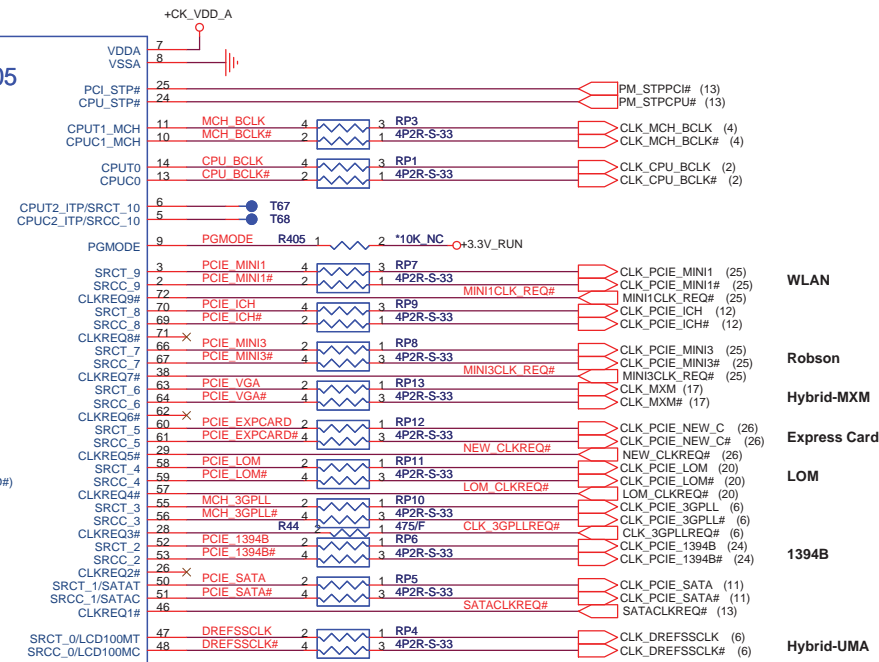
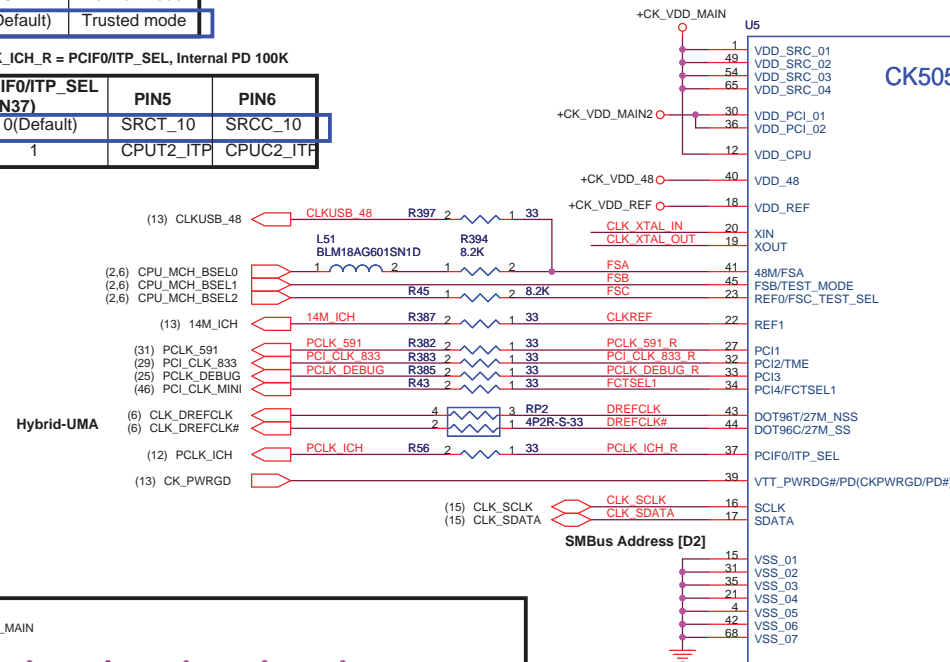


PGMODE R407 1 2 *10K NC

Populate for Napa platforms only.

Internal PU 100K

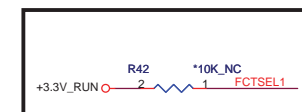
PGMODE	CLK mode	PIN9
0	CK410	VTT_PWRGD#/PD#
1(Default)	CK505	CK_PWRGD/PD#



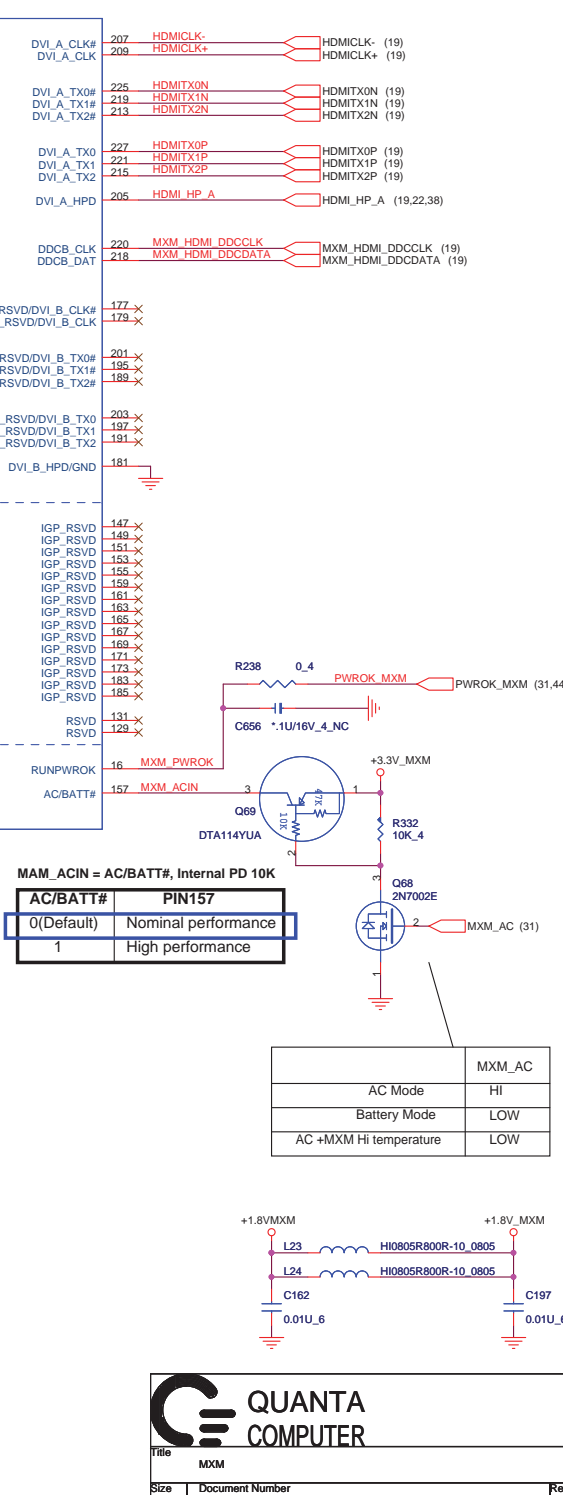
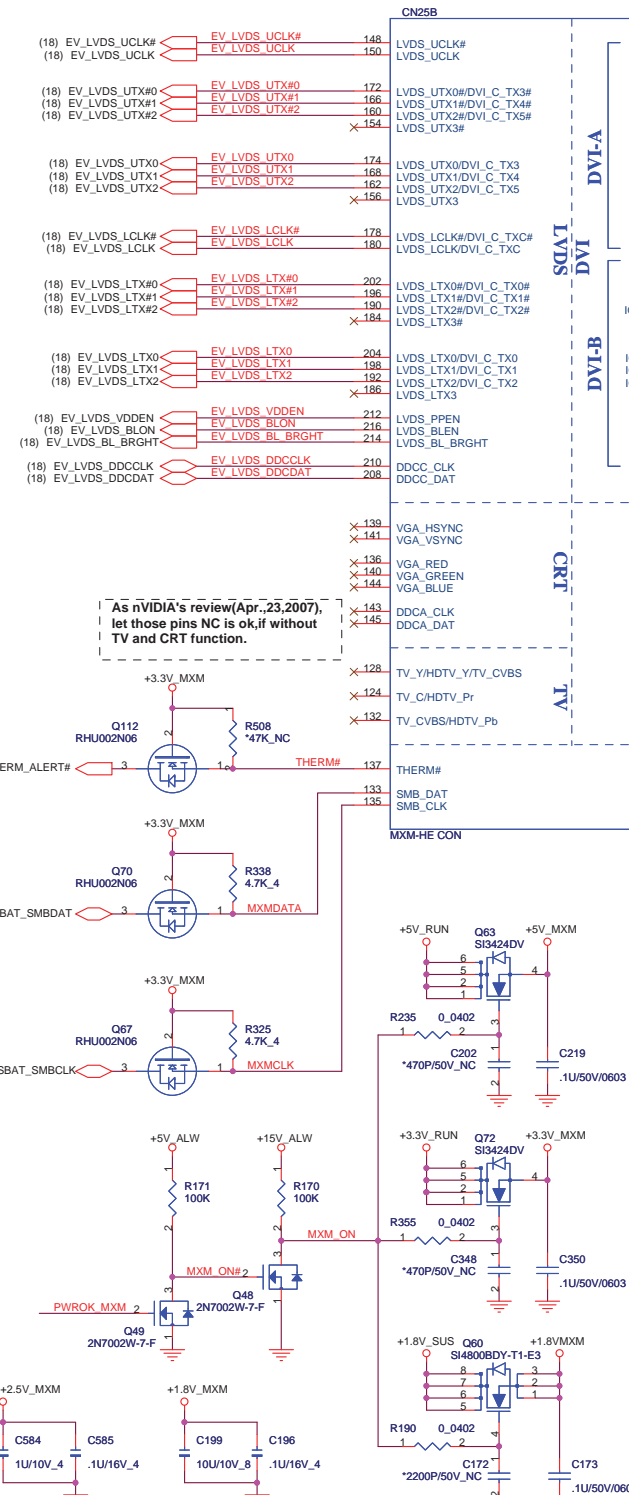
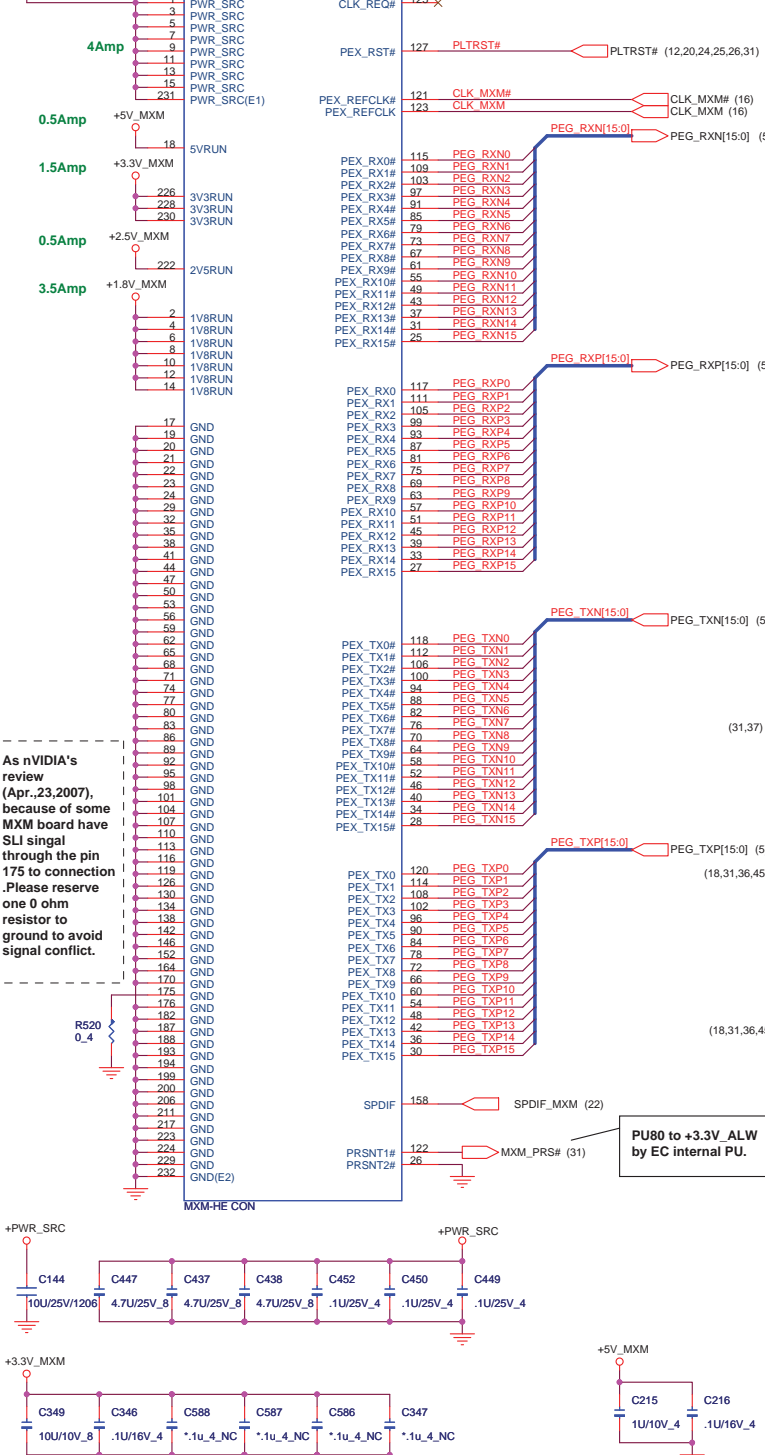
FCTSEL1 = PCI4/FCTSEL1, Internal PD 100K

PCI4/FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0 = UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Discrete	27M_NSS	27M_SS	SRCT0	SRCC0

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

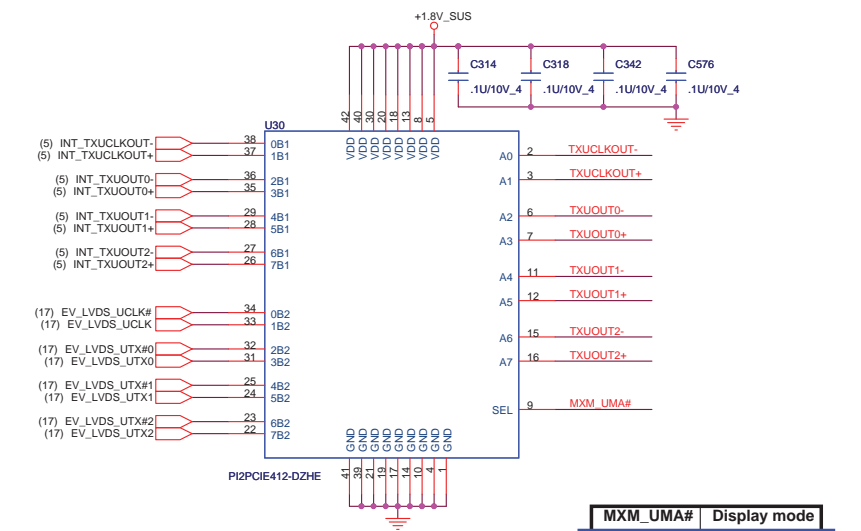
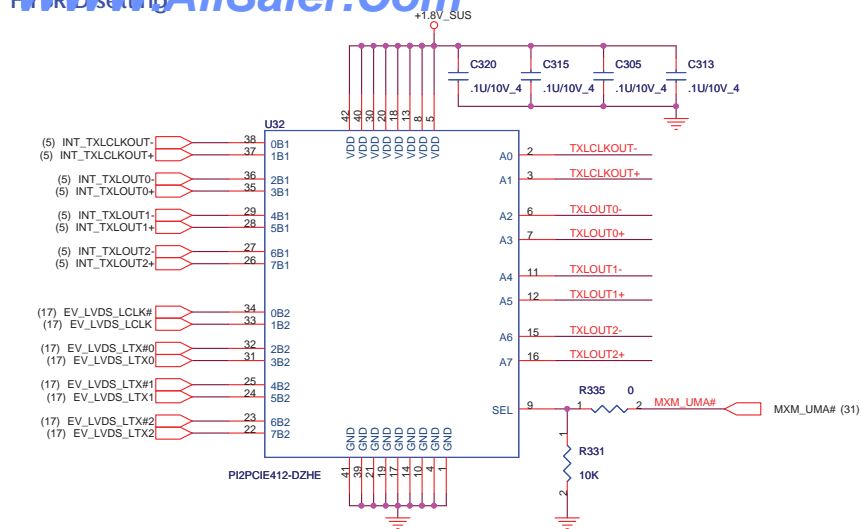


Title		Clock Generator
Size	Document Number MX3	Re

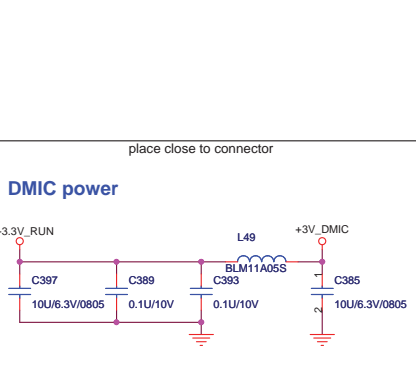
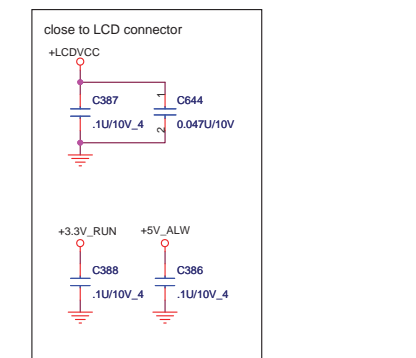
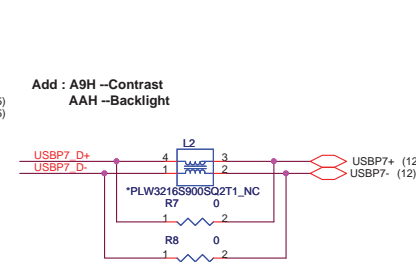
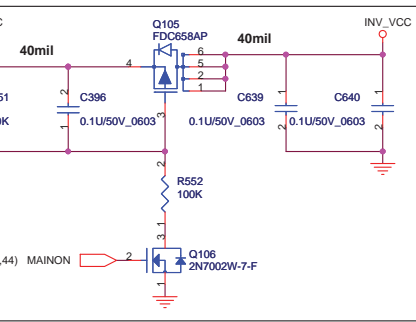
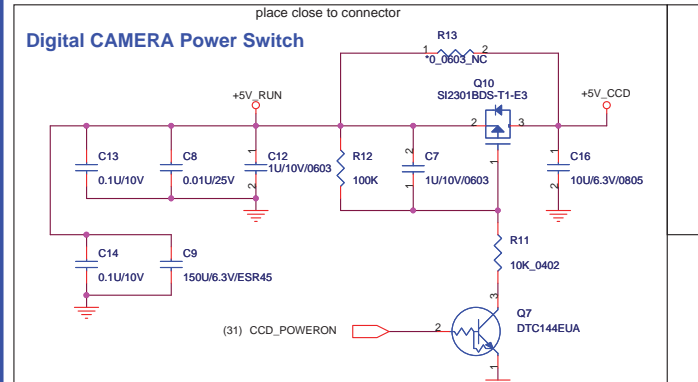
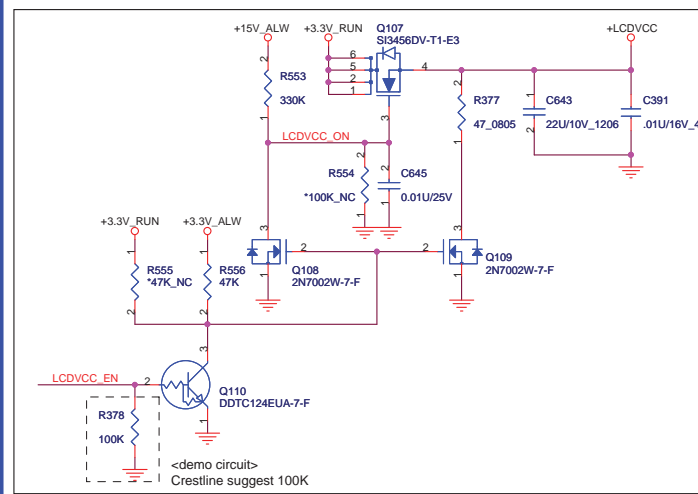
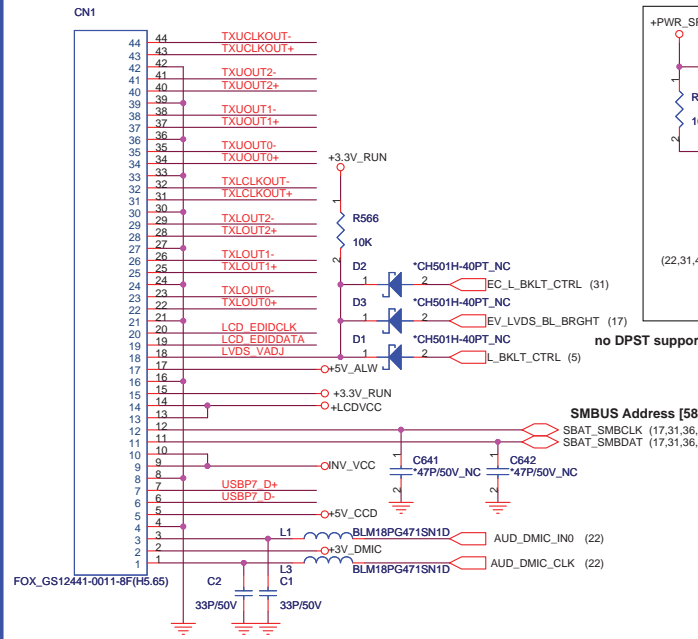
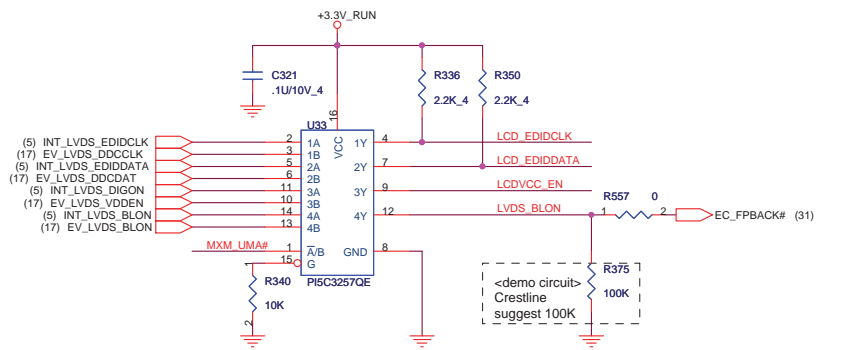


QUANTA COMPUTER

Title		MXM
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Rev		2C



MXM_UMA#	Display mode
0	Hybrid-UMA
1	Hybrid-MXM



QUANTA COMPUTER

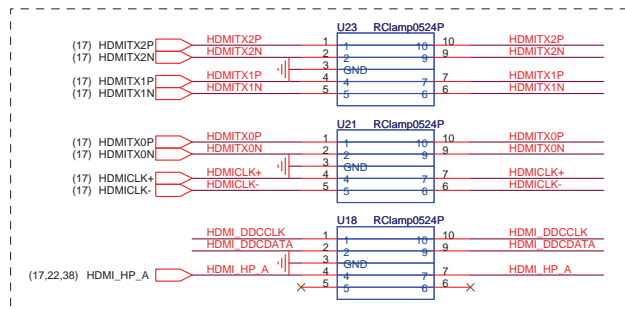
Title: LVDS/E-switch/CCD/DMIC

Size: Document Number MX3

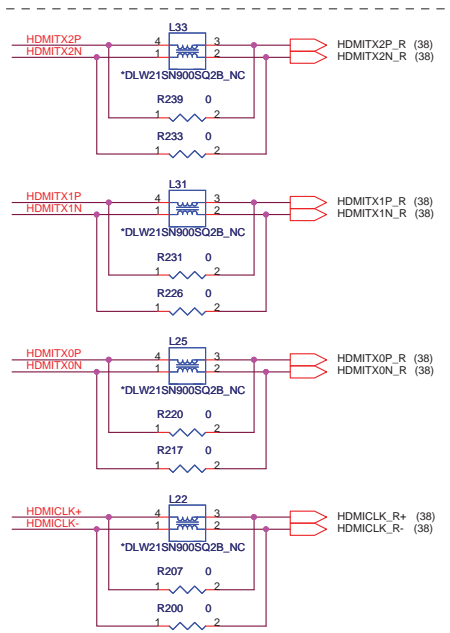
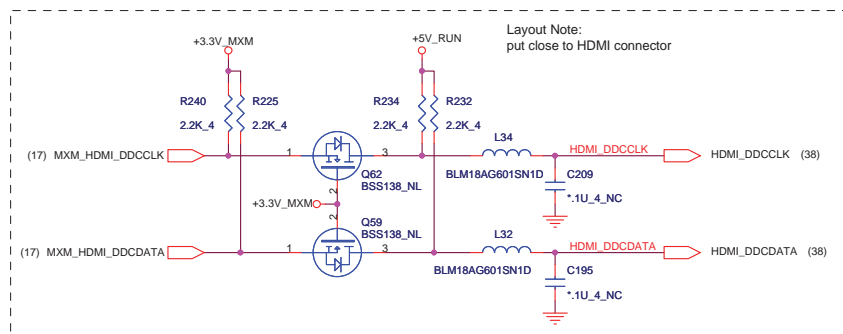
Date: Friday, October 12, 2007

Sheet: 18 of 53

Rev: 2A

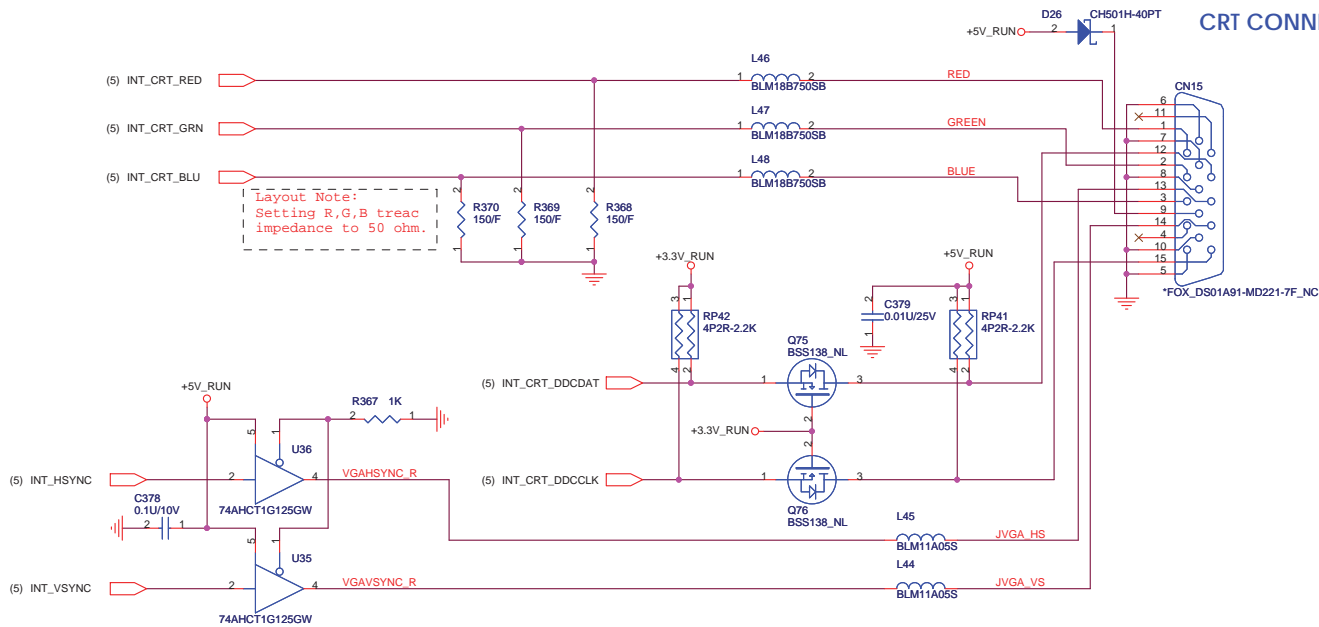


for ESD

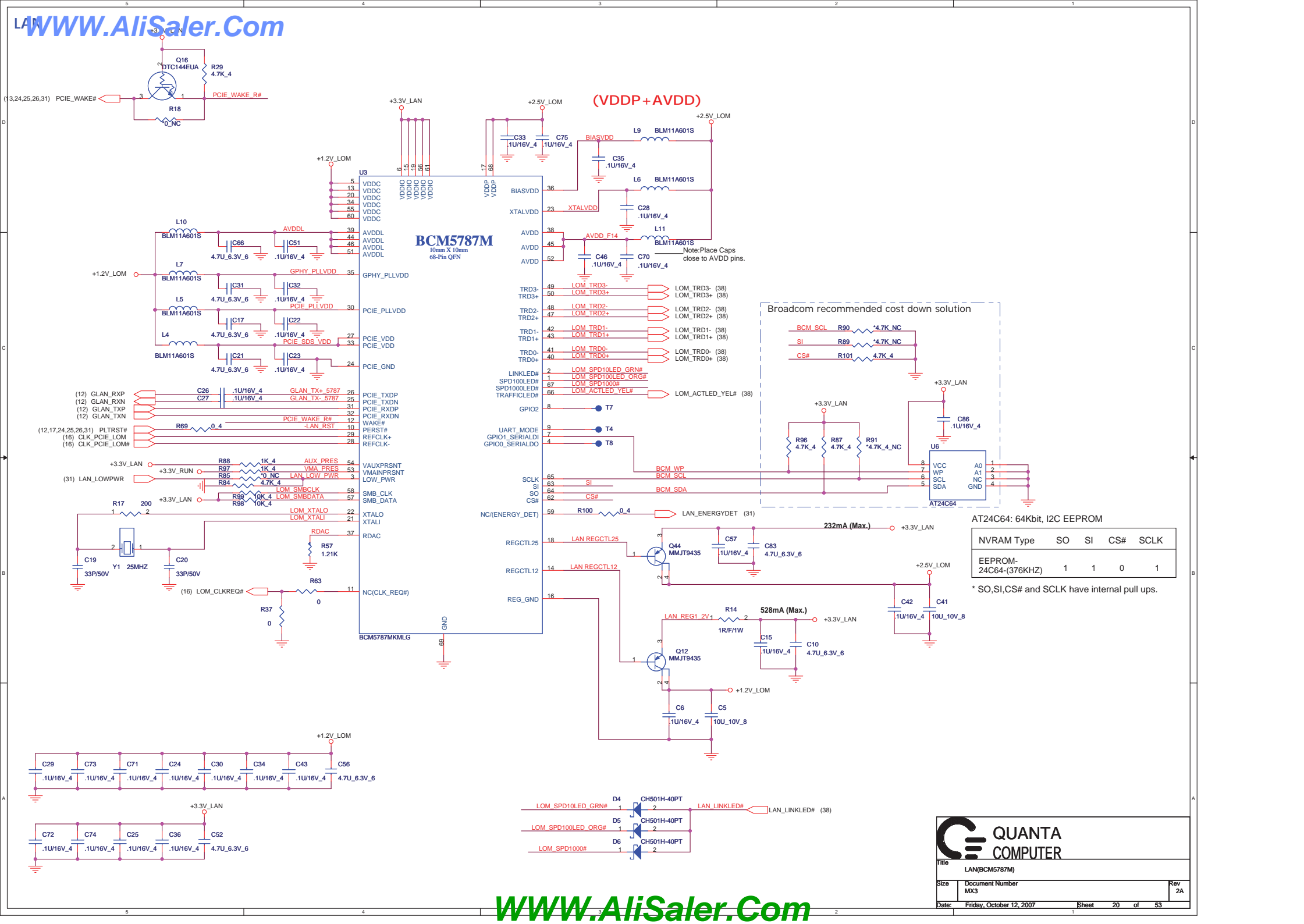


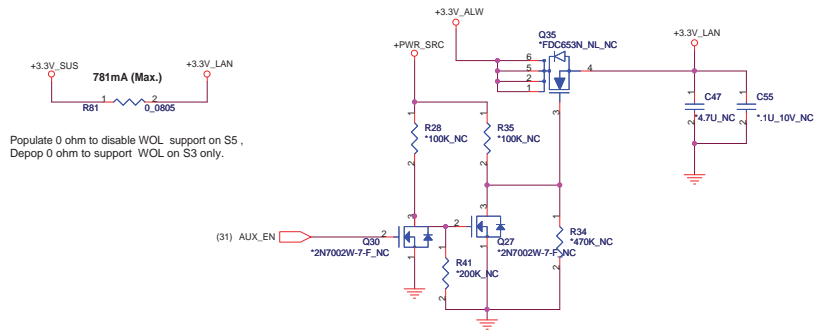
for EMI

CRT CONNECTOR FOR Debug

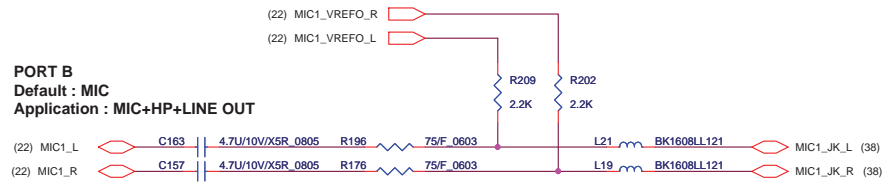


QUANTA COMPUTER	
Title: HDMI & CRT(for debug)	
Size: MX3	Document Number: Rev 2B
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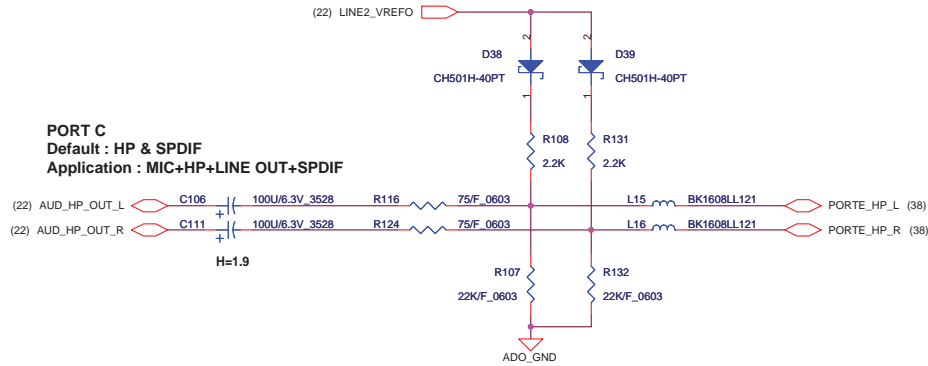


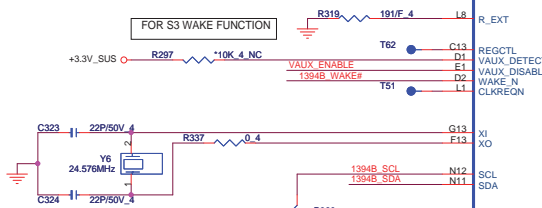
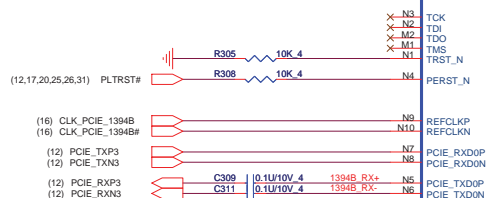
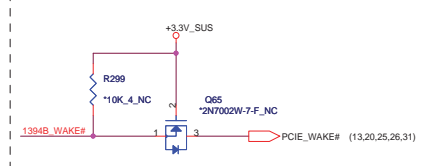
PORT B
Default : MIC
Application : MIC+HP+LINE OUT



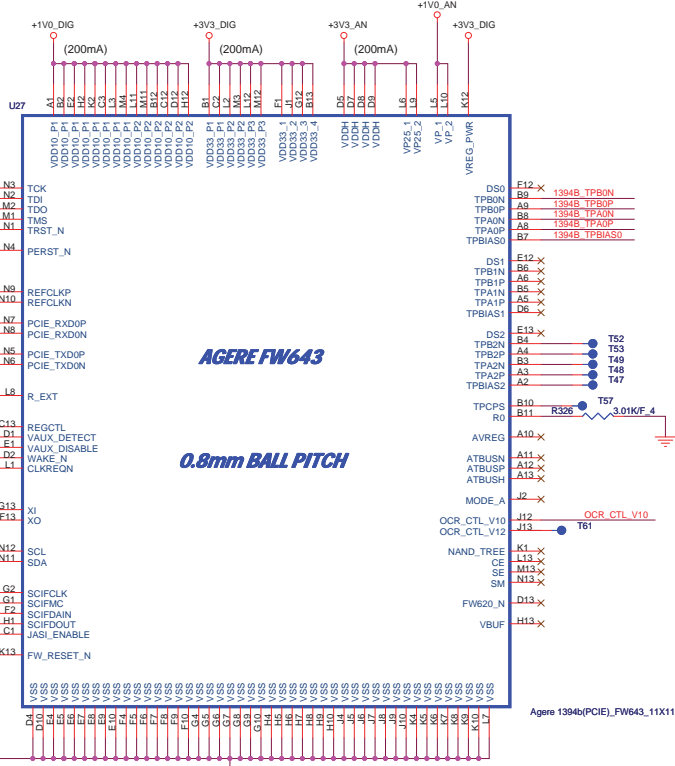
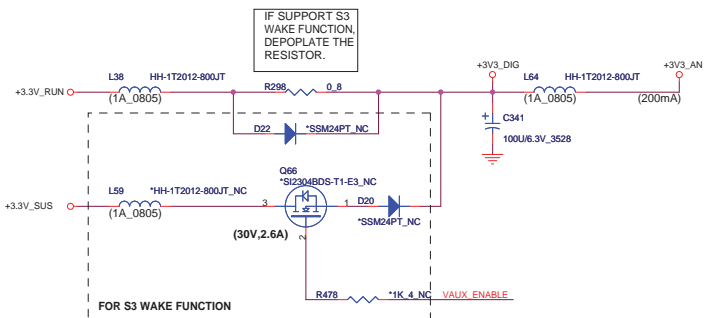
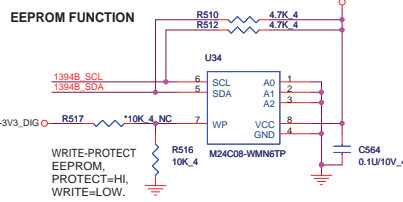
1. In order to meet Vista Premium requirements, MLCC input cap must use X5R dielectric material and 10V DC rated voltage.
2. If use polarity 100uF cap, then need to add 22K pull-down resistors.
3. R196, R176, R116, R124 are used for enhancing Audio quality and ESD ability.

PORT C
Default : HP & SPDIF
Application : MIC+HP+LINE OUT+SPDIF

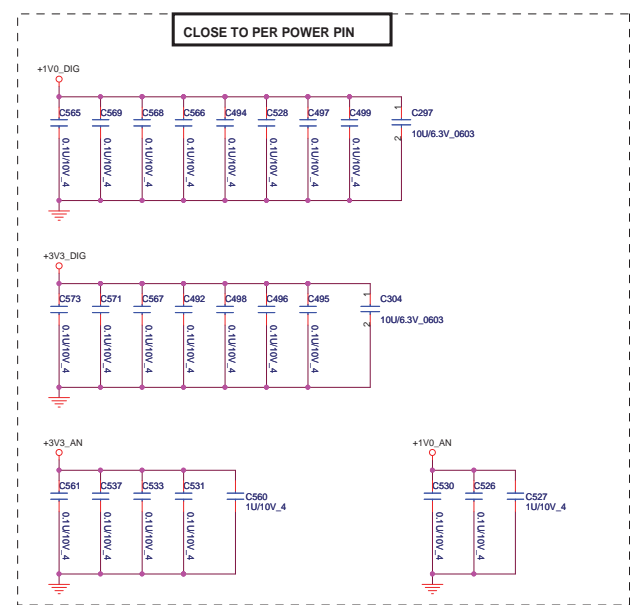
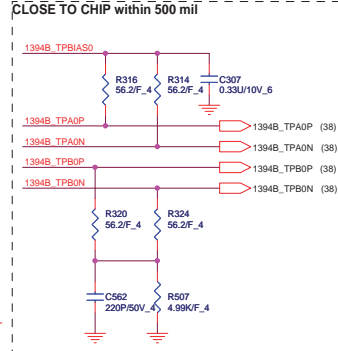




For FW643 rev03, EEPROM is not supported for code reading, pop this Res. For rev04, EEPROM is supported, depop this Res. Considering the cost saving, may pop this Res always for code reading from BIOS.



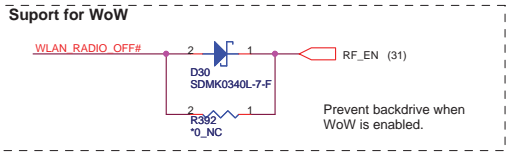
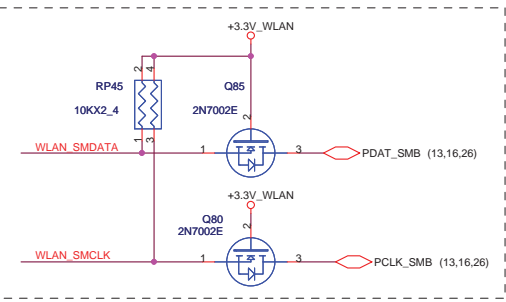
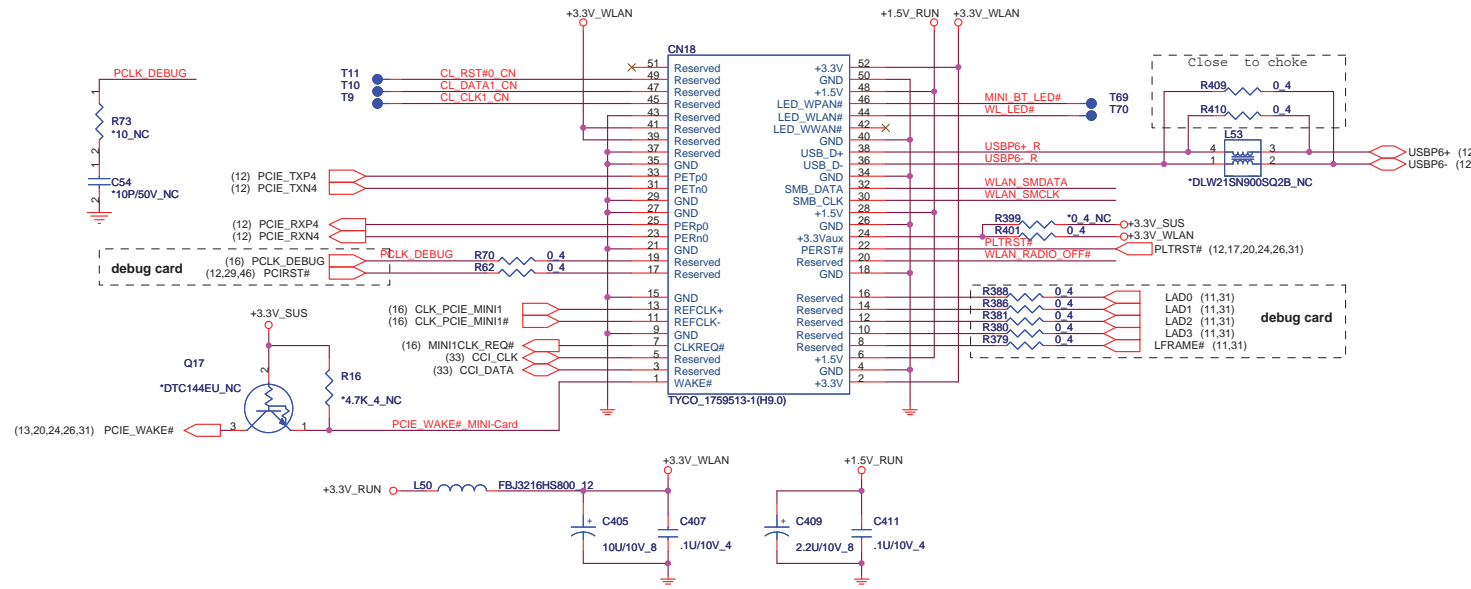
AGERE FW643
0.8mm BALL PITCH



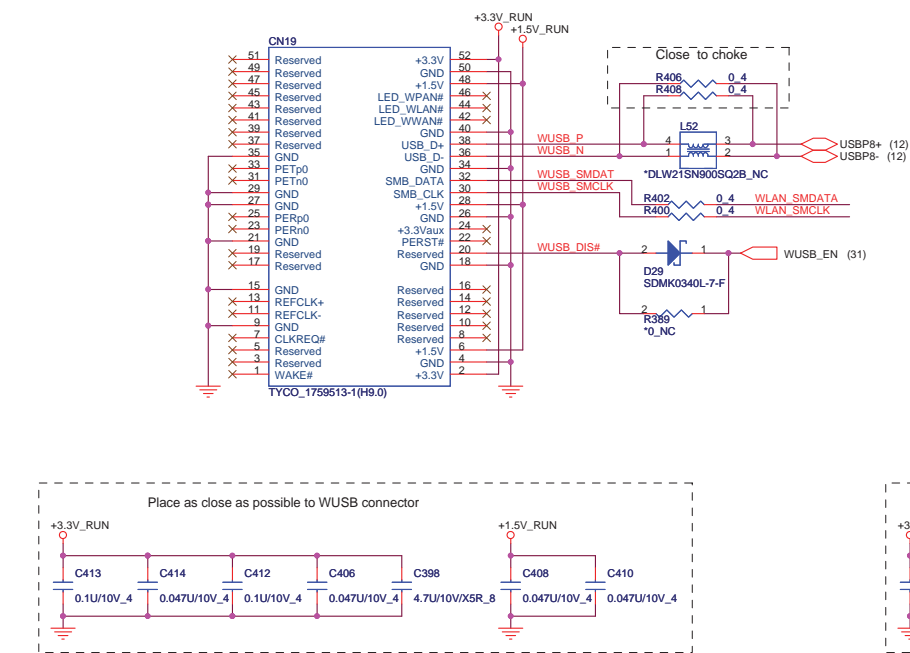
Note: Collector Pins on Transistor to be connected to CAPs using large heatsink 0.4 sq in on Top Side

Multiple Vias to DND

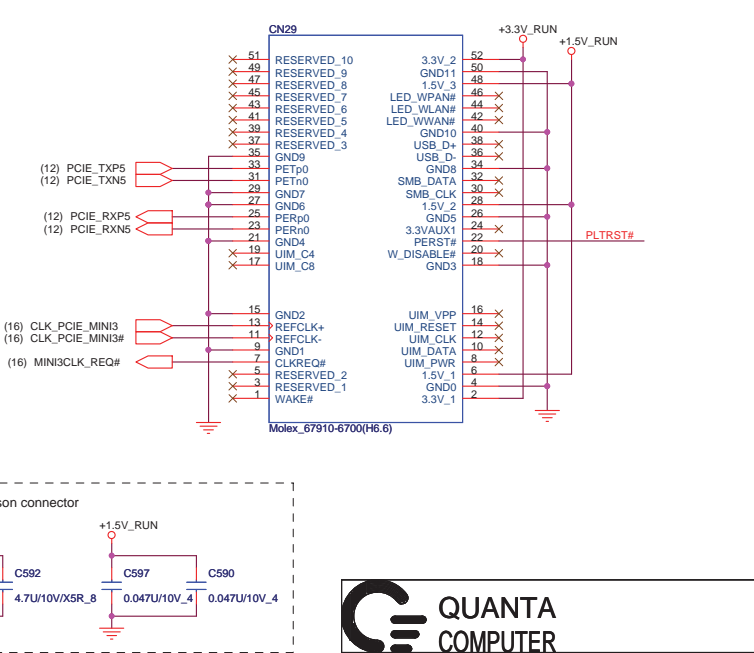
MiniCard connector - WLAN



MiniCard connector - Wireless-USB



MiniCard connector - Robson



QUANTA COMPUTER

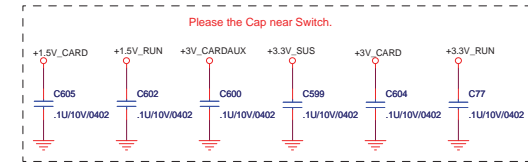
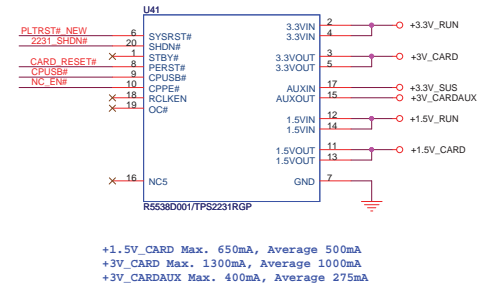
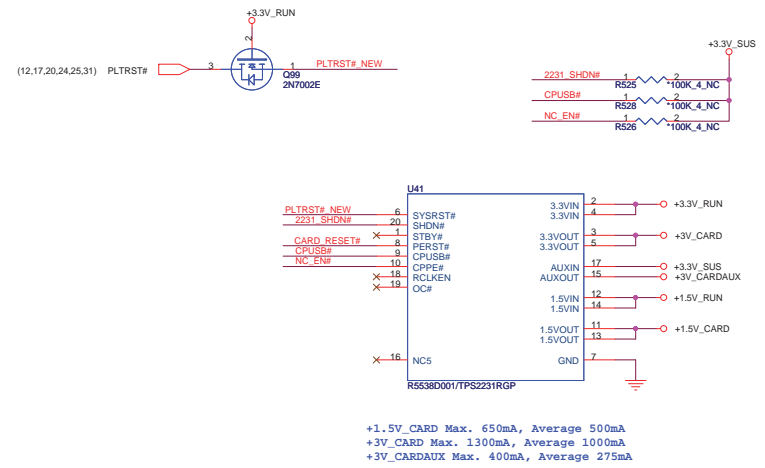
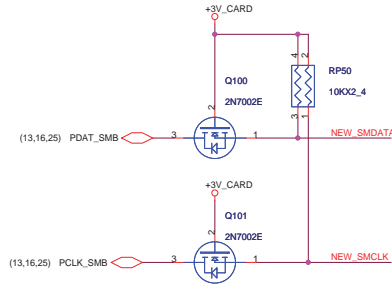
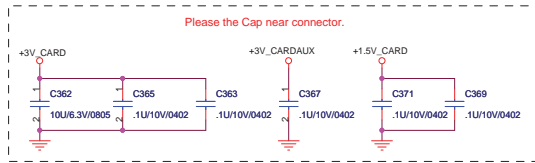
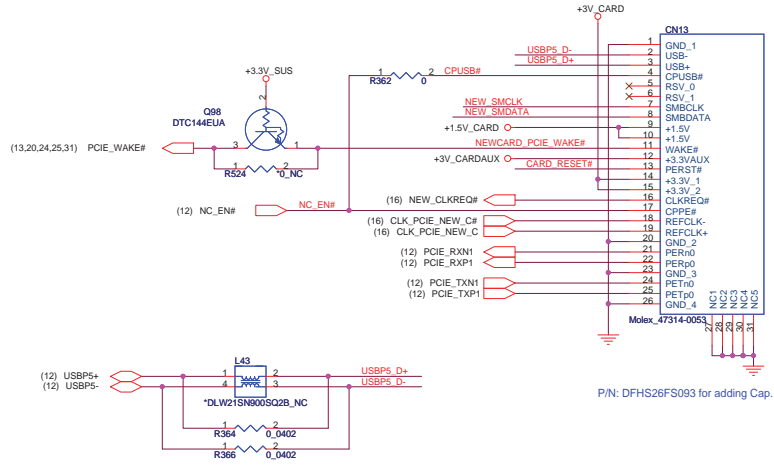
Title: Mini Card(WLAN/WUSB/Rob)

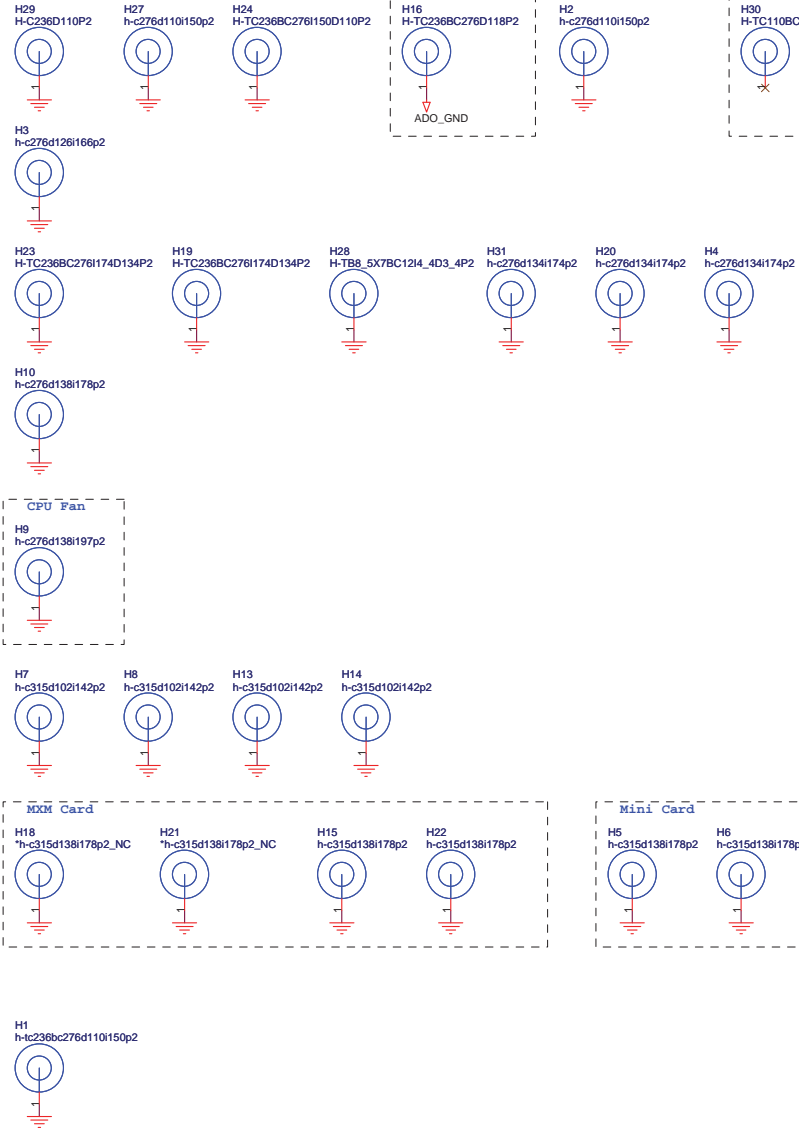
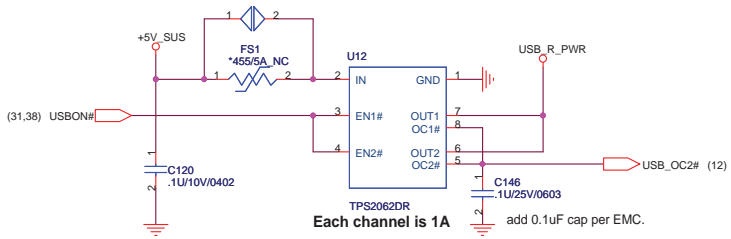
Size: MX3

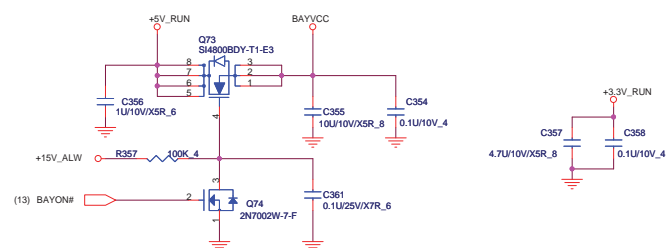
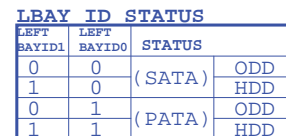
Document Number: 1A

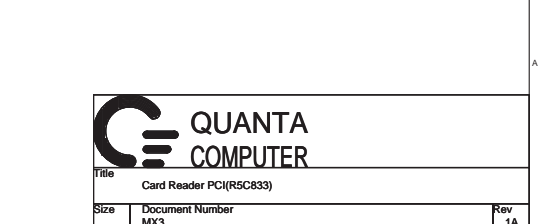
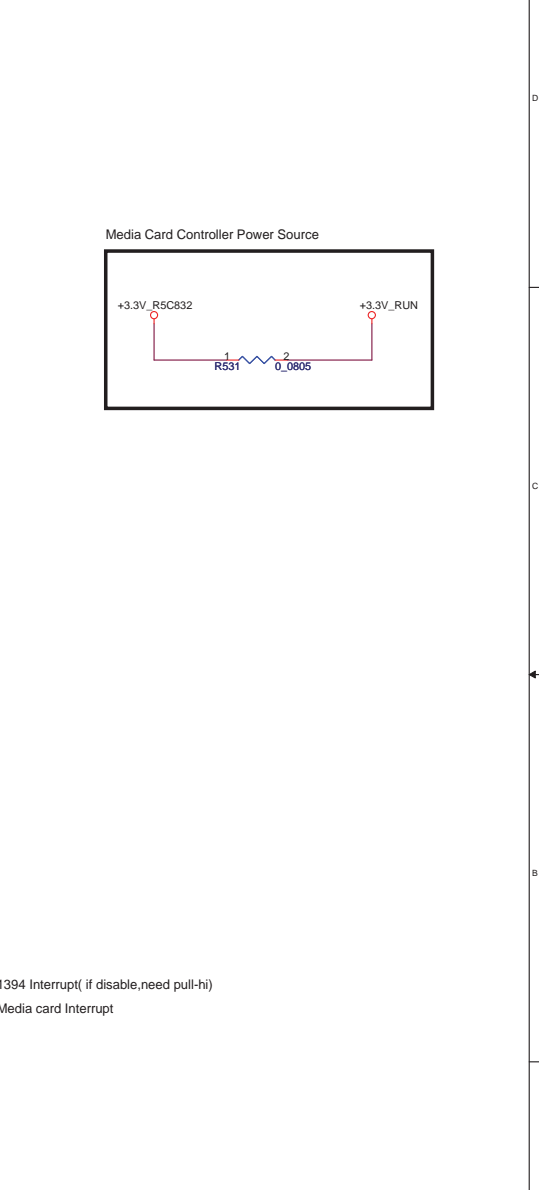
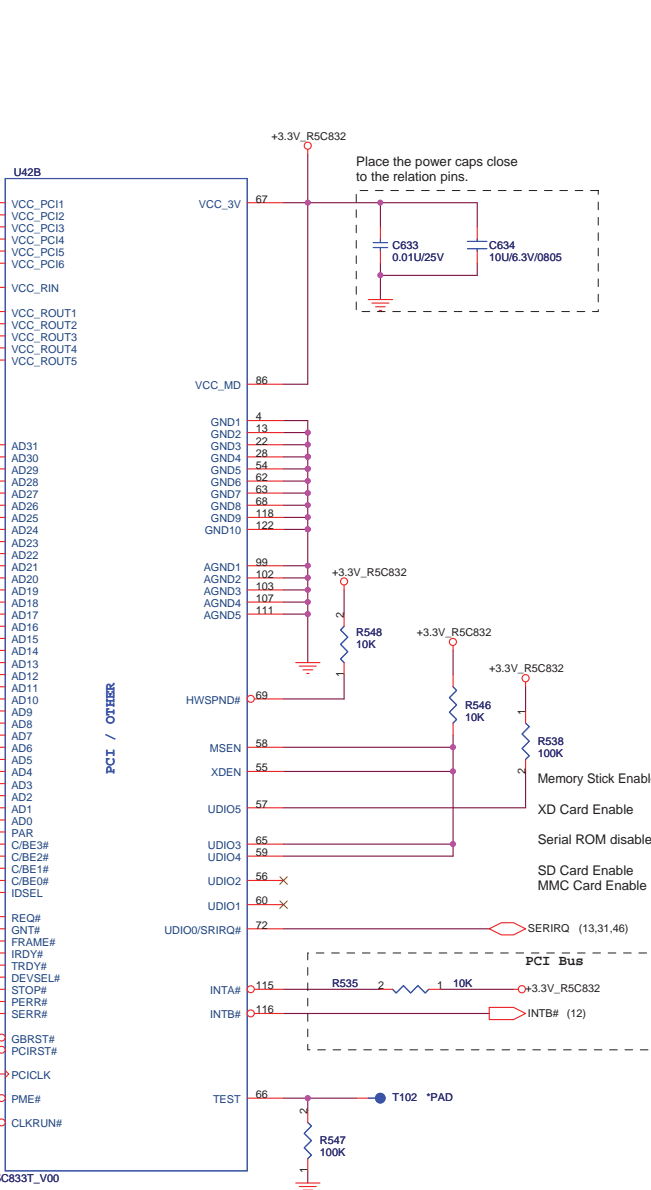
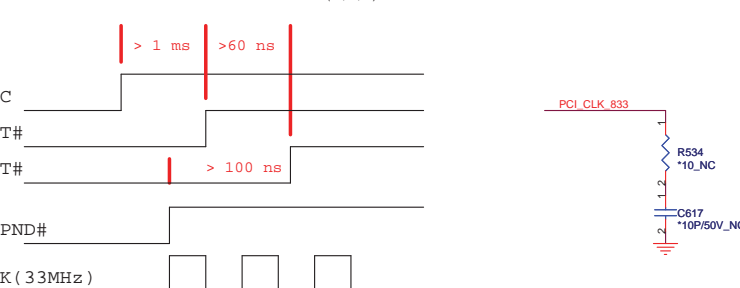
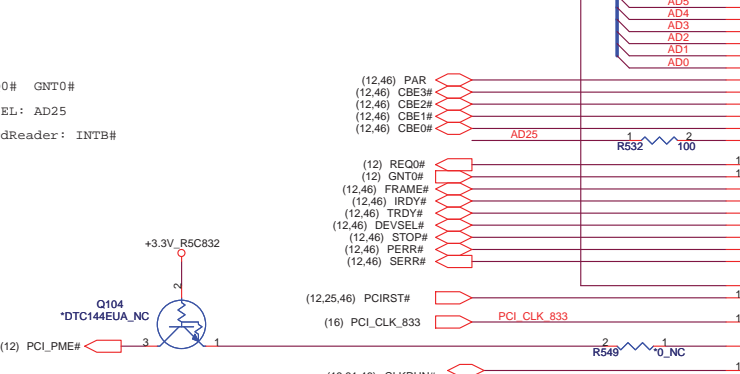
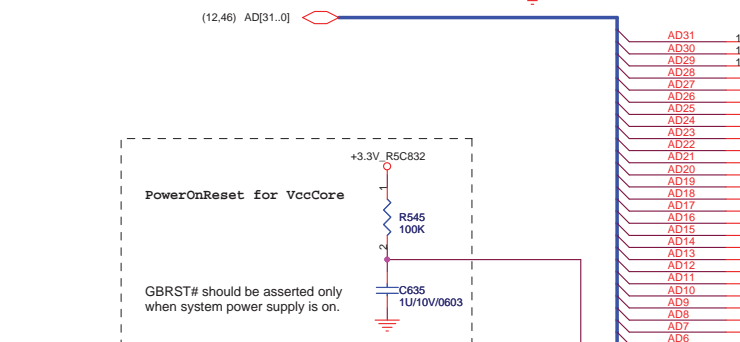
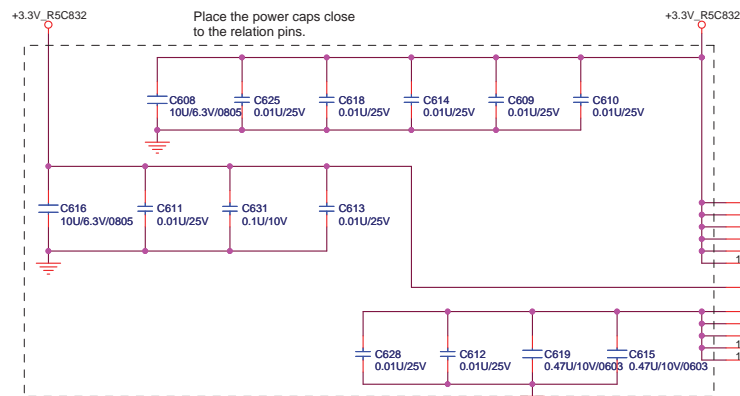
Date: Friday, October 12, 2007

Sheet: 25 of 53









QUANTA COMPUTER

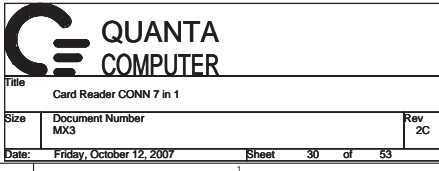
Title: Card Reader PCI(R5C833)

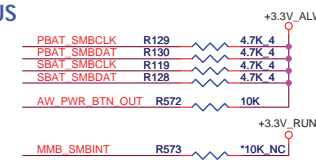
Size: Document Number MX3

Date: Friday, October 12, 2007

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Rev: 1A





I/O Address	
BADDR1-0	Index Data
0 0	XOR TREE TEST MODE
0 1	CORE DEFINED
1 0	2Eh 2Fh
1 1	164Eh 164Fh

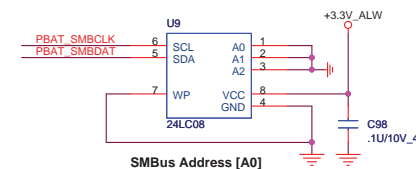
SHBM=0: Enable shared memory with host BIOS

BADDR0 CCD_POWERON R212 10K 4

BADDR1 SOUT_CR_DEBUG R211 *10K 4

SHBM RF_EN R169 10K 4

1/13 Confirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware



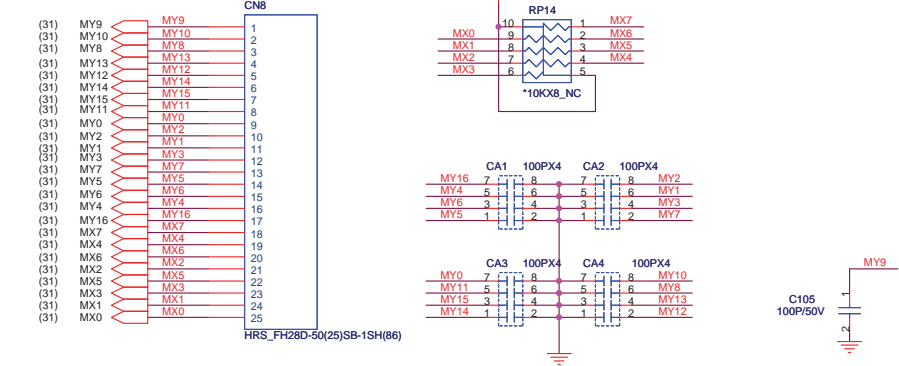
1/13 Confirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)

JEN0# = CHG_SBATT, JENK# = MY0; Internal PU(30K) for JEN0#, PU(80K) for JENK#

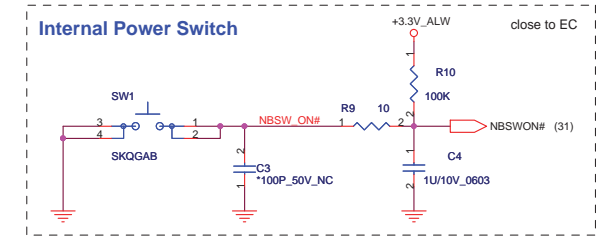
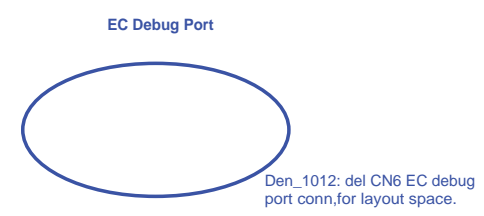
JEN0# (Pin 24)	JENK# (Pin 53)	Functionality of Pins 17, 20, 21, 23, 25, 27	Functionality of Pins 47, 48, 50, 51, 52
1 (Default)	1 (Default)	GPIO Port signals	Keyboard Scan output
0	1	JTAG signals	Keyboard Scan output
1	0	GPIO Port signals	JTAG signals
0	0	Illegal Strap	Combination



Title			
EC(WPC8769LDG)			
Size	Document Number	Rev	
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Date:	Friday, October 12, 2007	Sheet	31 of 53

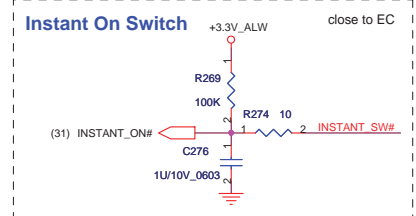
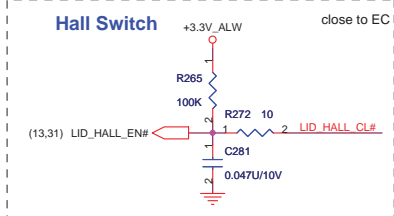
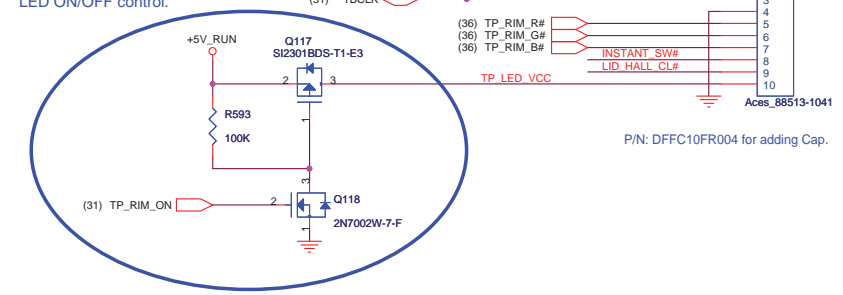


DEBUG PORT

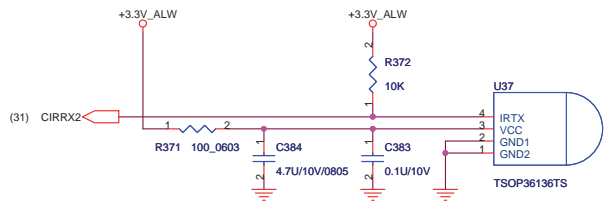


T/P

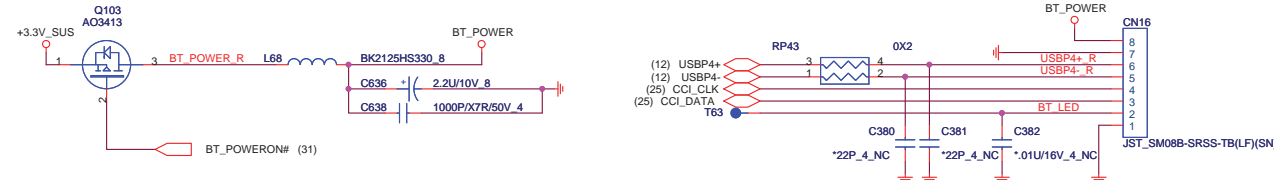
Den_1012: add for TP LED ON/OFF control.

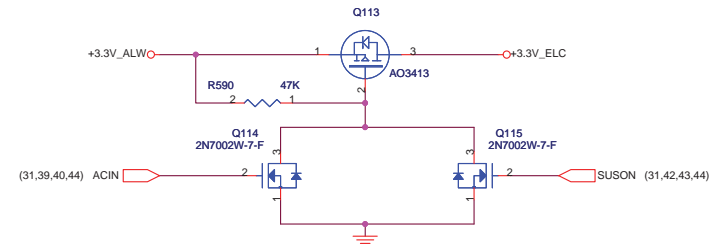
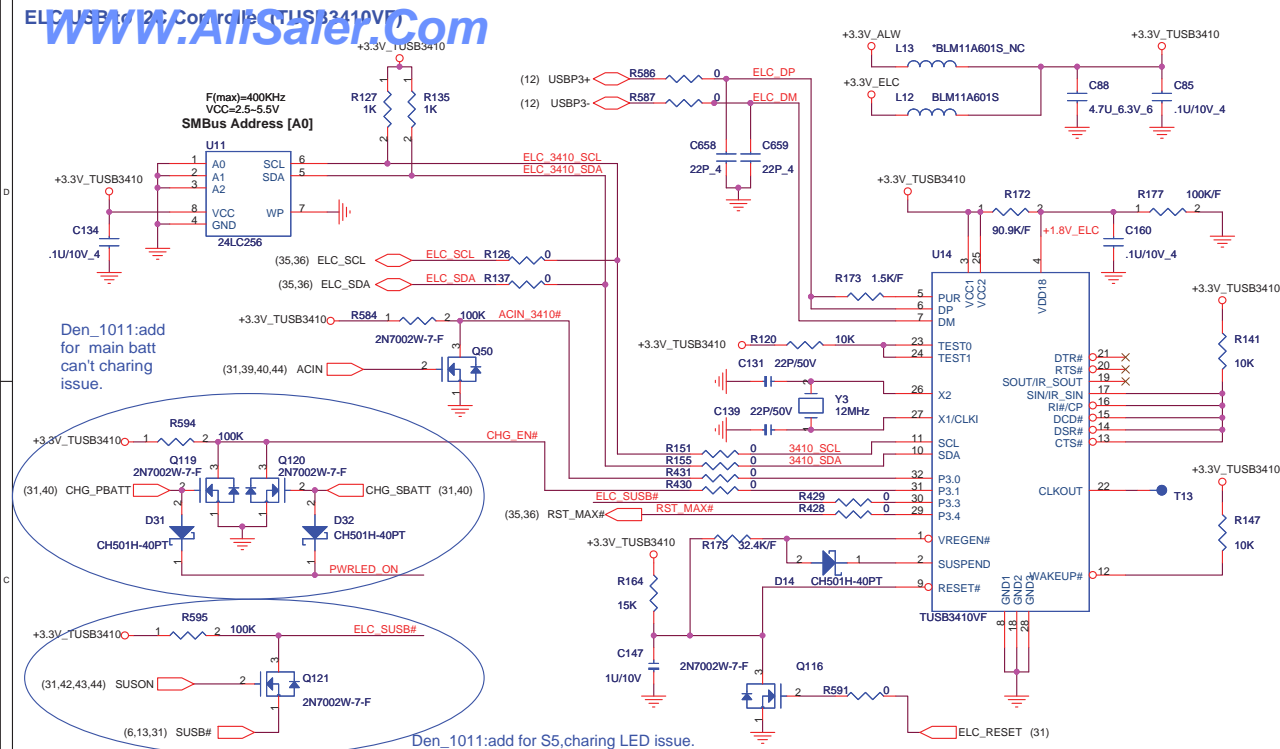


CIR module

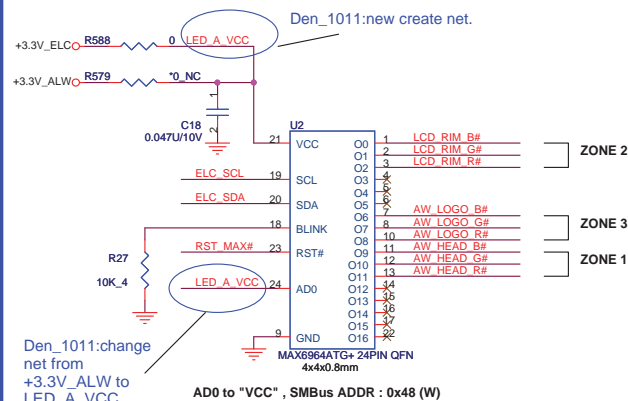


BLUETOOTH MODULE CONNECTOR



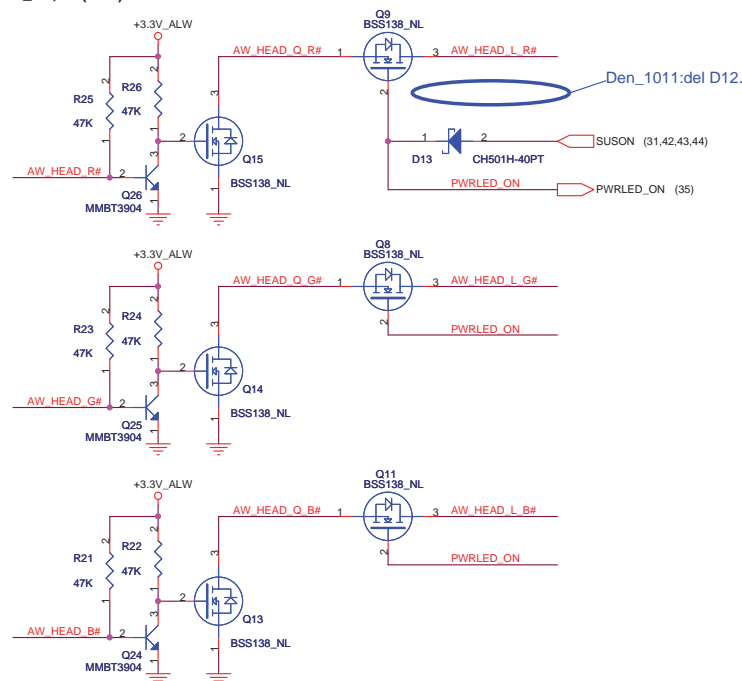


ZONE 1,2,3 --- ELC Controller (LCD Panel, A-Cover)



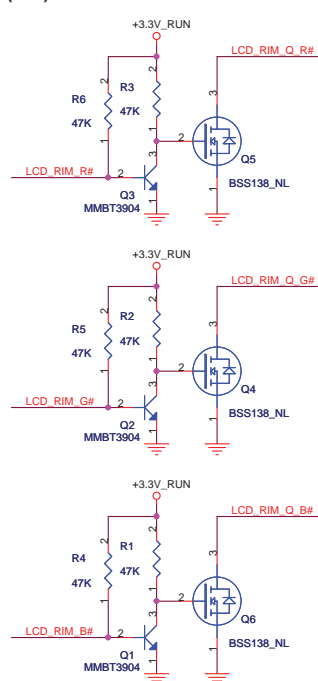
ZONE 1 --- AW Head Buffer (A-Cover, RGB LED*3)

BSS138_NL, ID (max) = 0.22A

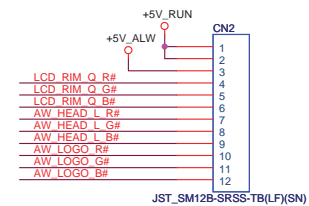


ZONE 2 --- LCD RIM Buffer (A-Cover, RGB LED*4)

BSS138_NL, ID (max) = 0.22A



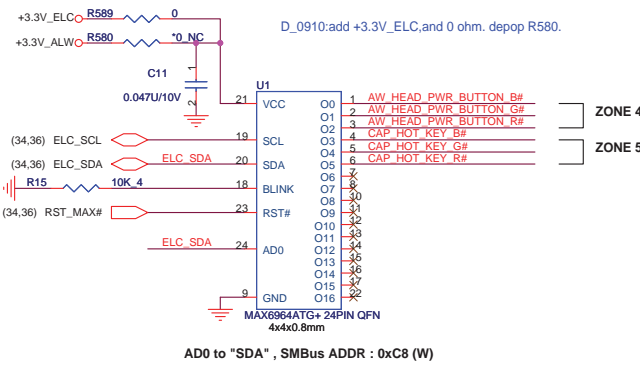
LED Connector (12 Pins) --- MB to LCD Panel (A-Cover)



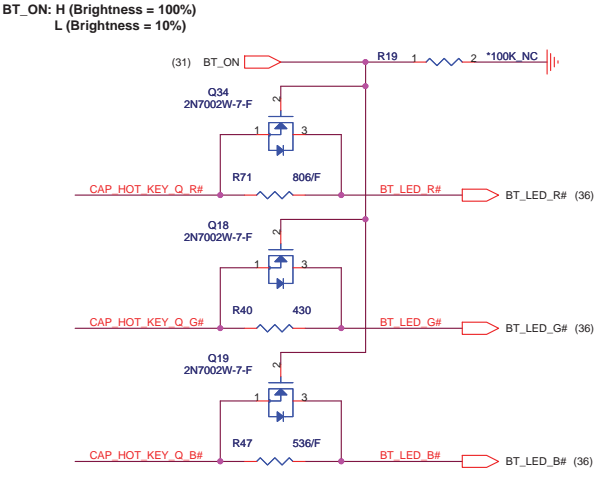
**ZONE 3 --- AW Logo
(A-Cover, RGB LED*2)**



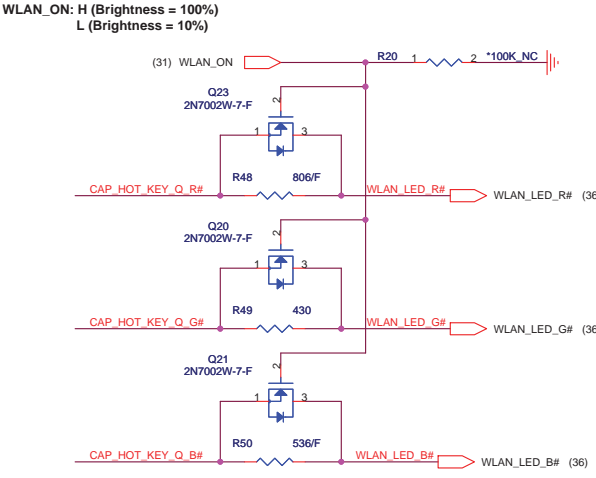
Title				ELC TUSB3410VF & ZONE 1-3			
Size	Document Number						Rev
	MX3						3
Date:	Friday, October 12, 2007			Sheet	34	of	53



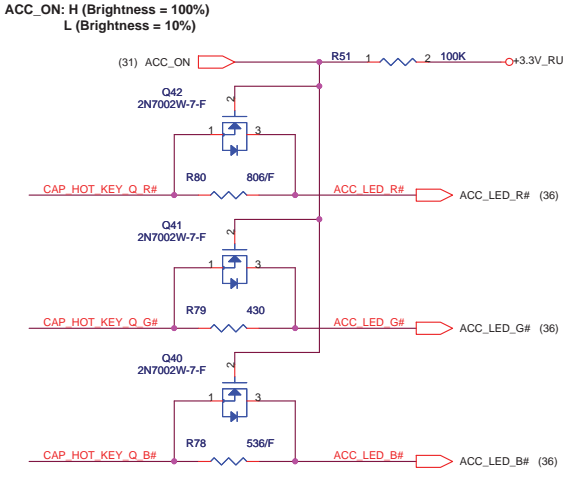
ZONE 5 --- BT (Bluetooth) LED



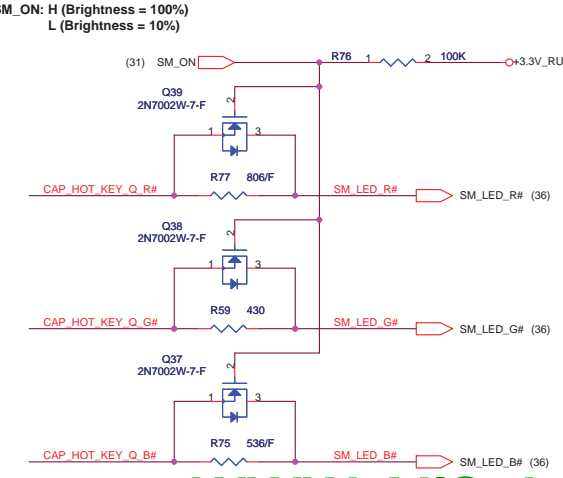
ZONE 5 --- WLAN (Wireless LAN) LED



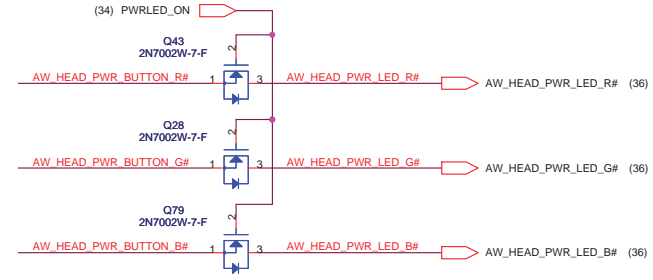
ZONE 5 --- ACC (Alienware command center) LED



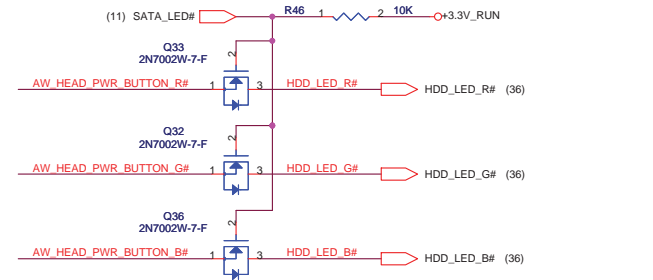
ZONE 5 --- SM (Silent Mode) LED



ZONE 4 --- Power Status--AW_Head_RIM (C-Cover, RGB LED*1)



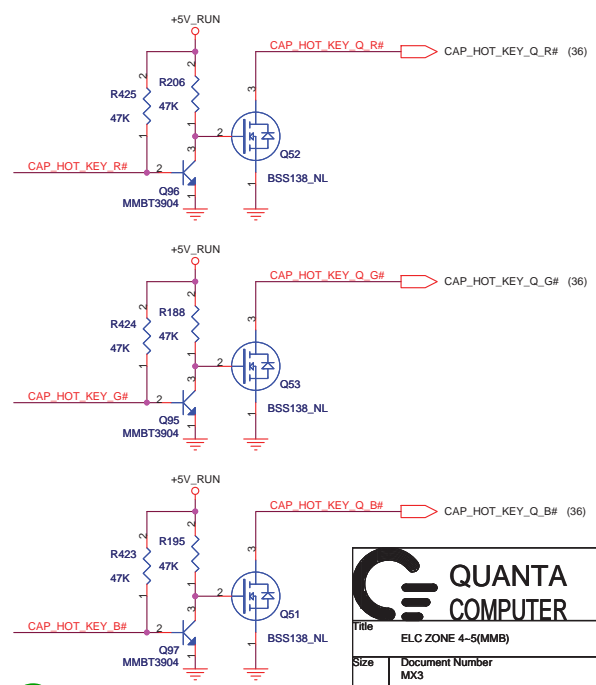
ZONE 4 --- HDD ACT--AW_Head_Eyes (C-Cover, RGB LED*1)



ZONE 5 --- LED Buffer (C-Cover, RGB LED*7)

- 1.MMB Right -- BT/WLAN/ACC/SM (RGB LED*4)
- 2.MMB Left -- Caps/Num/Scroll Lock (RGB LED*3)

BSS138_NL, ID (max) = 0.22A



QUANTA COMPUTER

Title: ELC ZONE 4-5(MMB)

Size: MX3

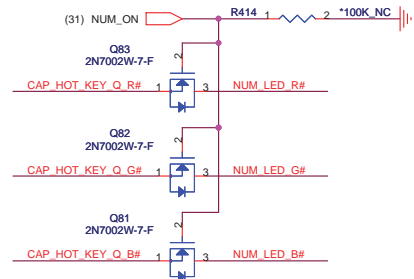
Document Number: MX3

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Rev: 2C

ZONE 6 - NUM (Num Lock) LED

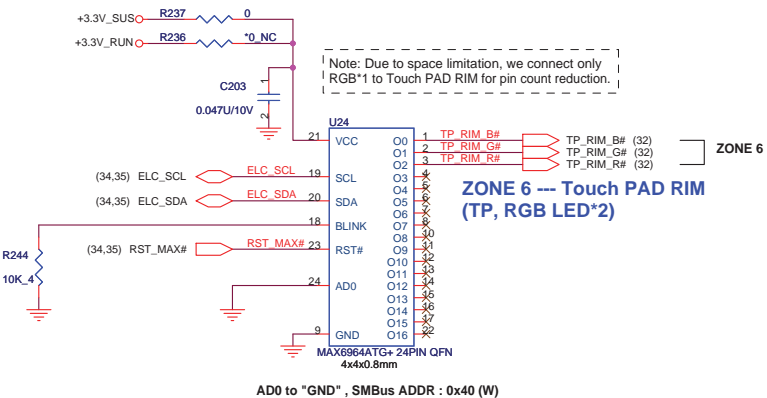


MMB CONN (42Pins)

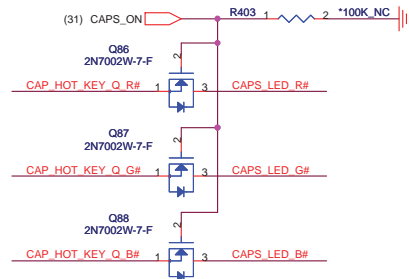


ZONE 6 --- ELC Controller (Touch PAD RIM)

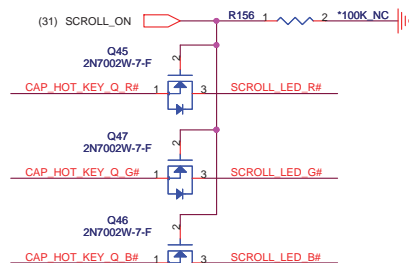
Note: LED Vendor: EVERLIGHT
P/N:12-23A/R6GHBHC-A01/2D



ZONE 5 --- CAPS (Caps Lock) LED

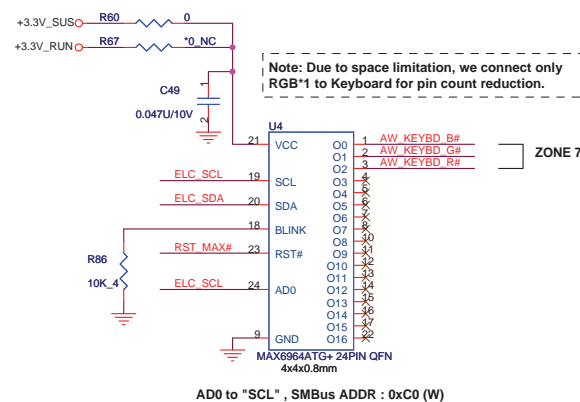


ZONE 5 --- SCROLL (Scroll Lock) LED

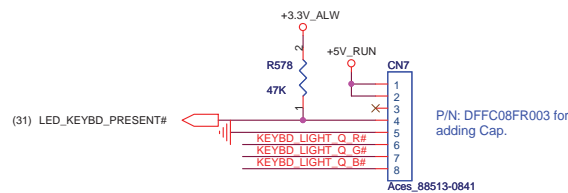


ZONE 7 --- ELC Controller (Keyboard)

Note: LED Vendor: EVERLIGHT
P/N:12-23A/R6GHBHC-A01/2D

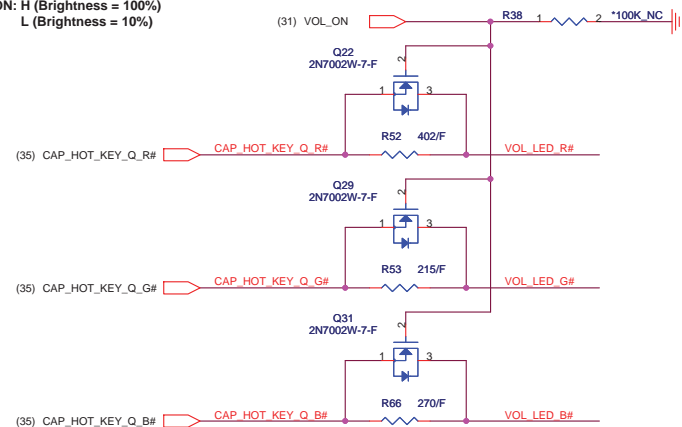


LED Connector (8 Pins) --- MB to Keyboard



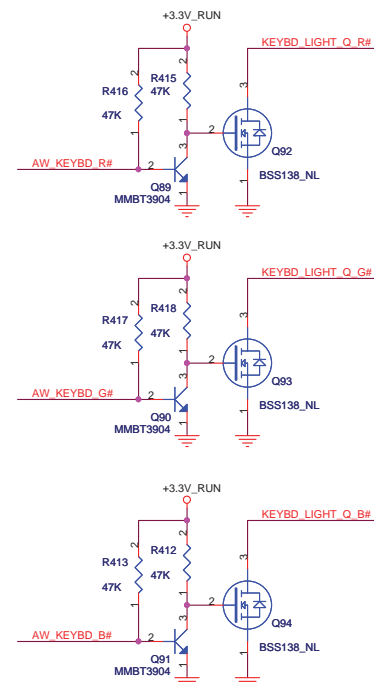
ZONE 5 --- VOL (Volumn Slider) LED

VOL_ON: H (Brightness = 100%)
L (Brightness = 10%)



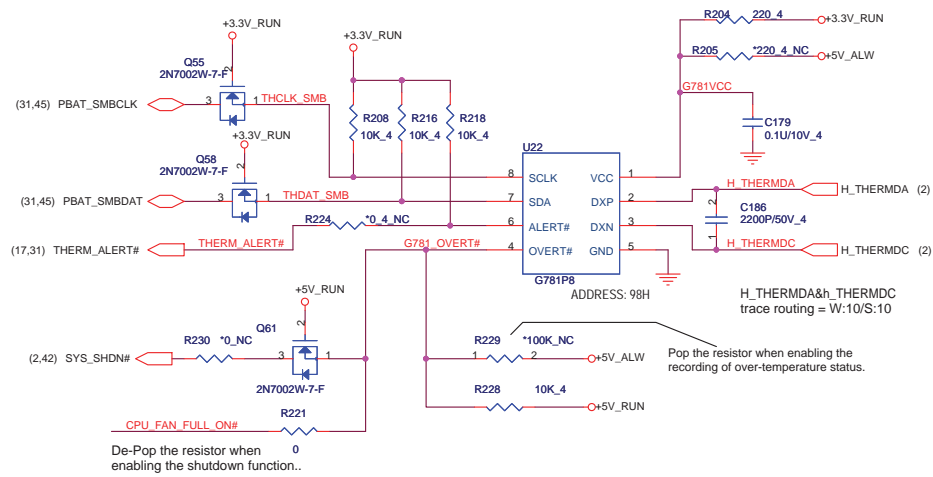
ZONE 7 --- Keyboard Buffer (KB, RGB LED*9)

BSS138_NL, ID (max) = 0.22A



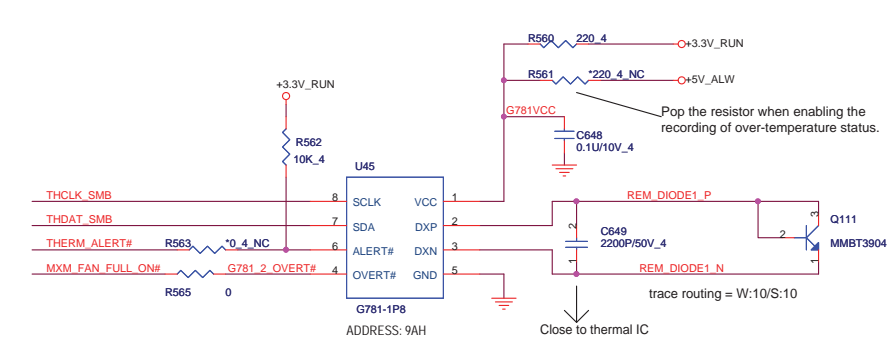
Title			
ELC ZONE 5-7(MMB,TP,KB)			
Size	Document Number	Rev	
	MX3	2	
Date:	Friday, October 12, 2007	Sheet	36 of 53

A: FOR CPU TEMP.
B: MB SKIN TEMP (CPU SIDE)



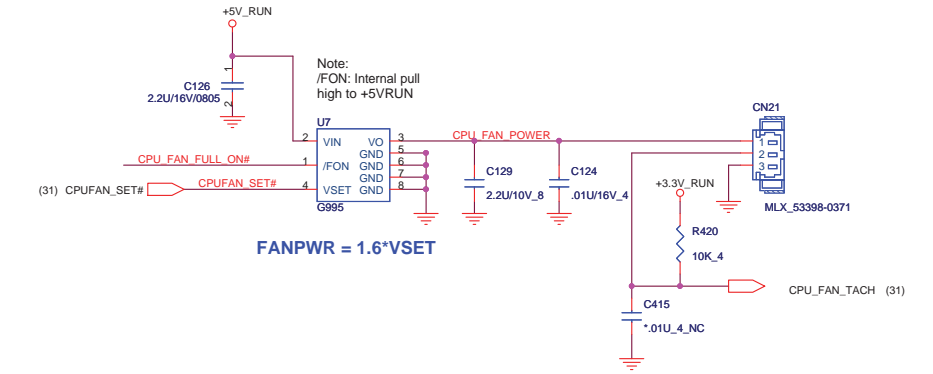
Note: The Over-Temperature flags stay high until cleared by POR, or until the status byte register is read.

C: FOR MXM MODULE TEMP.
D: MB SKIN TEMP (MXM MODULE)



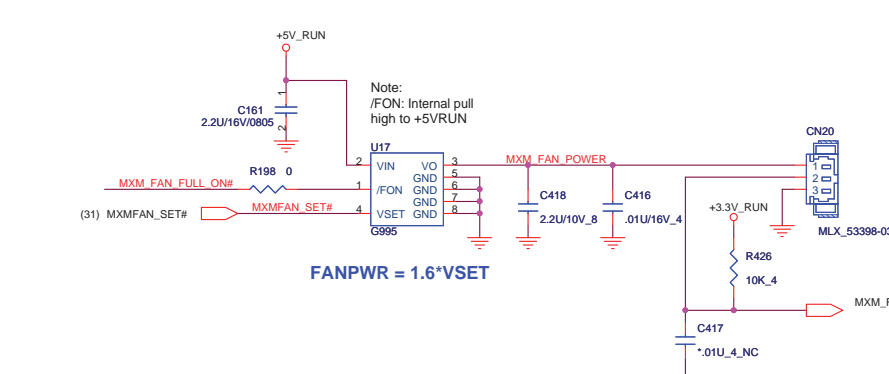
Note: The Over-Temperature flags stay high until cleared by POR, or until the status byte register is read.

CPU FAN



FANPWR = 1.6*VSET

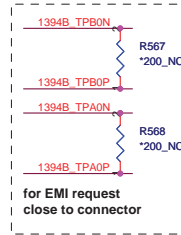
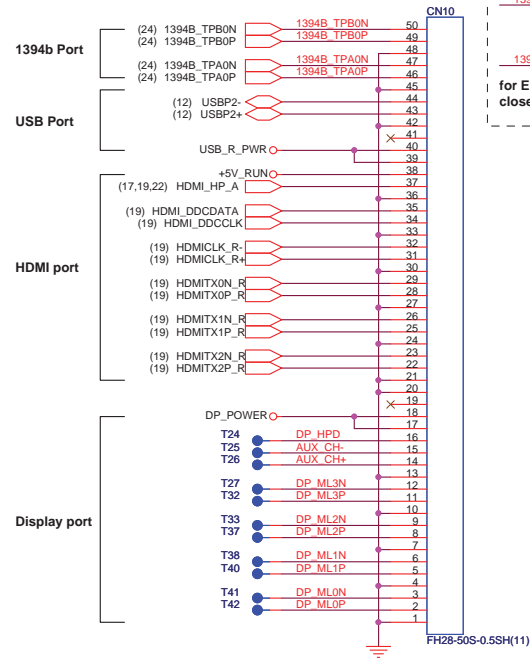
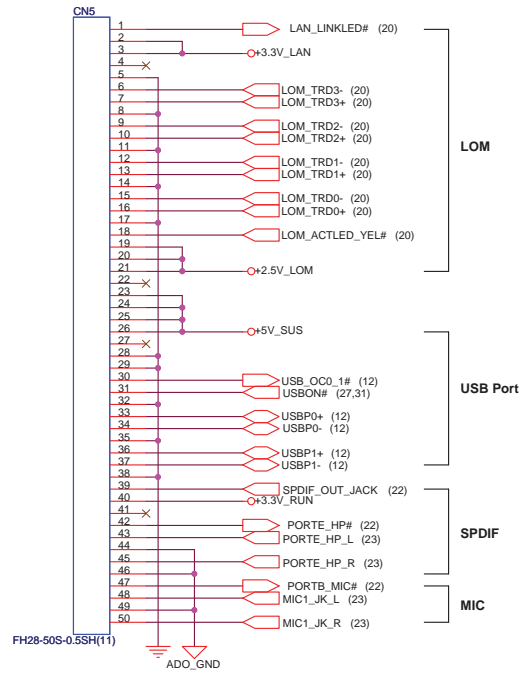
MXM FAN

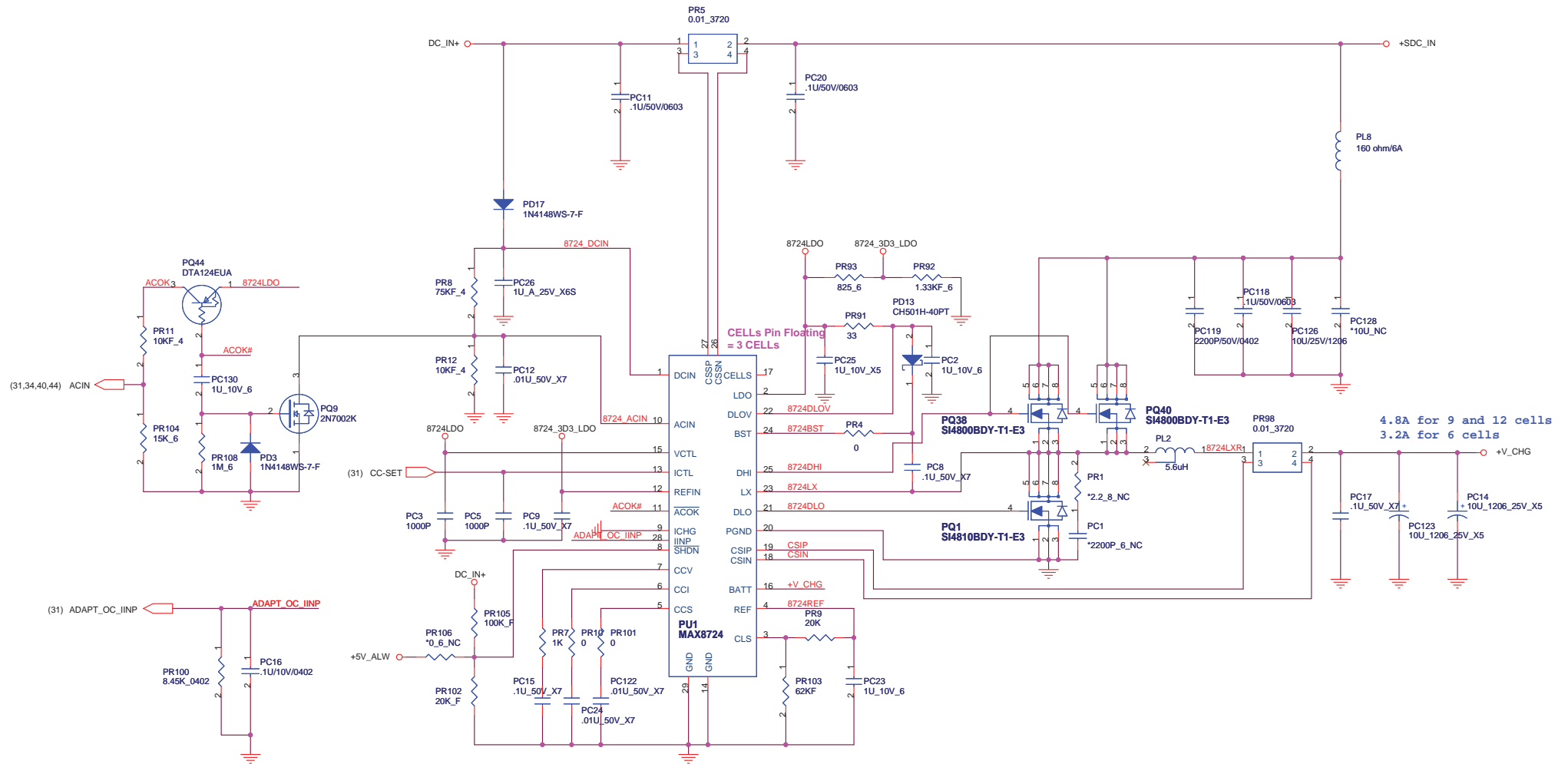


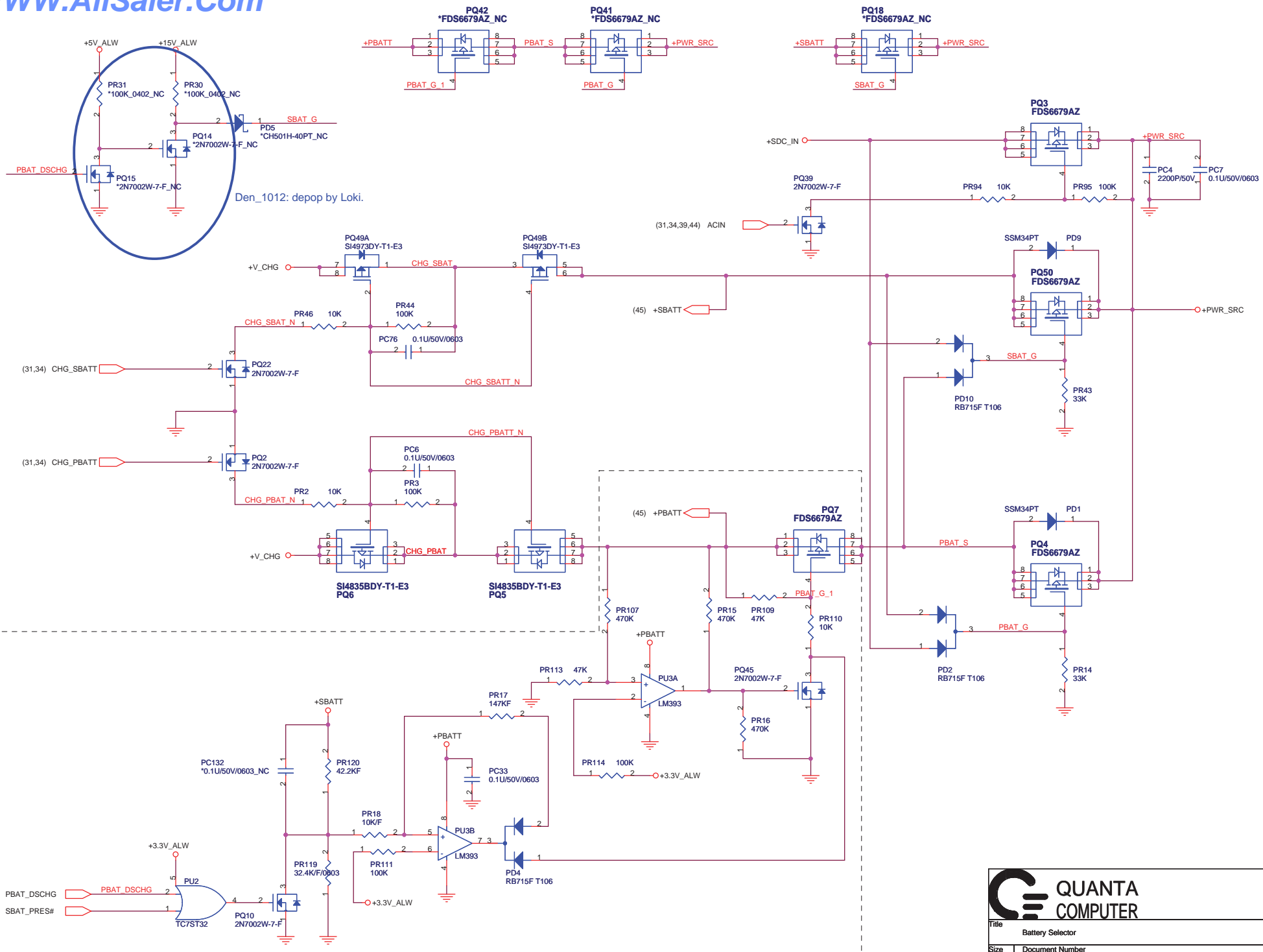
FANPWR = 1.6*VSET

to AUDIO board connector

to HDMI board connector





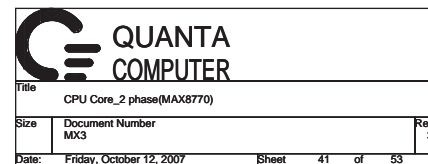


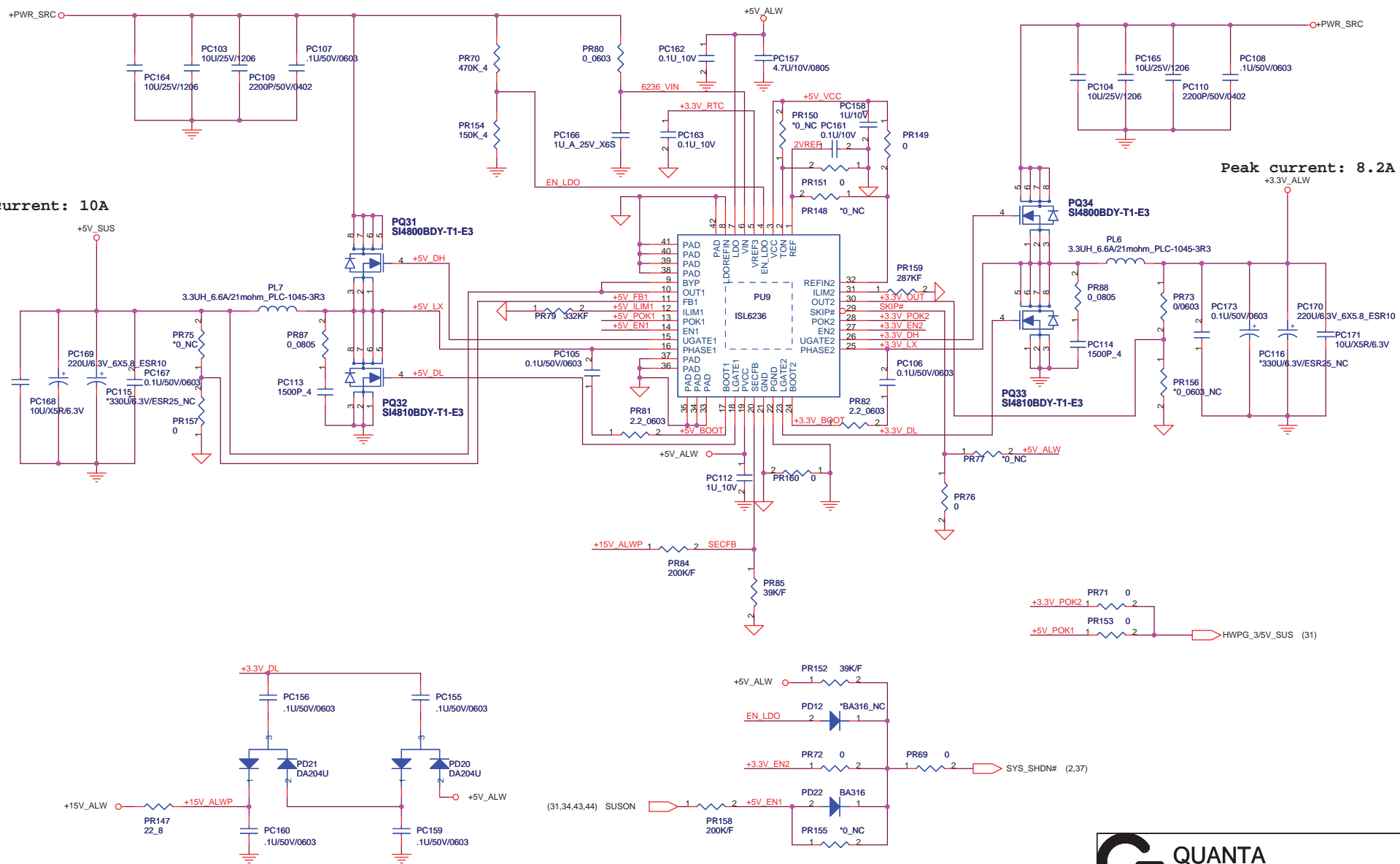
QUANTA COMPUTER

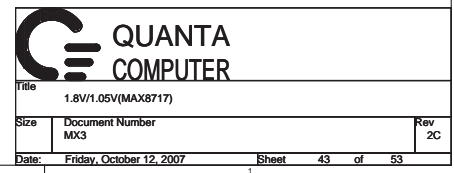
Title: Battery Selector

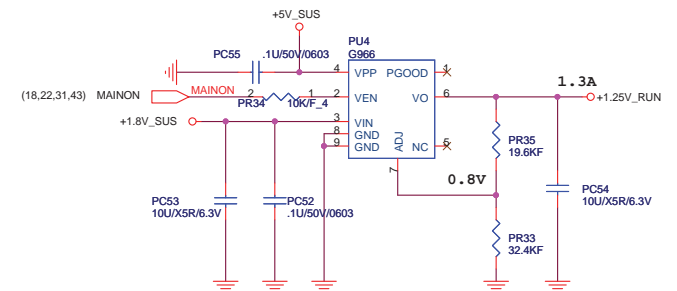
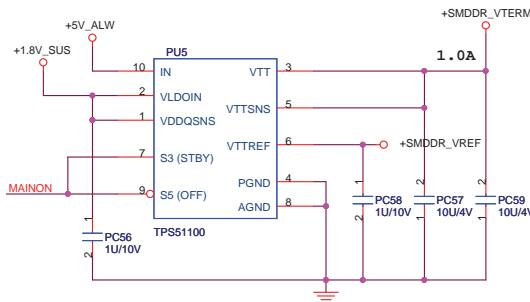
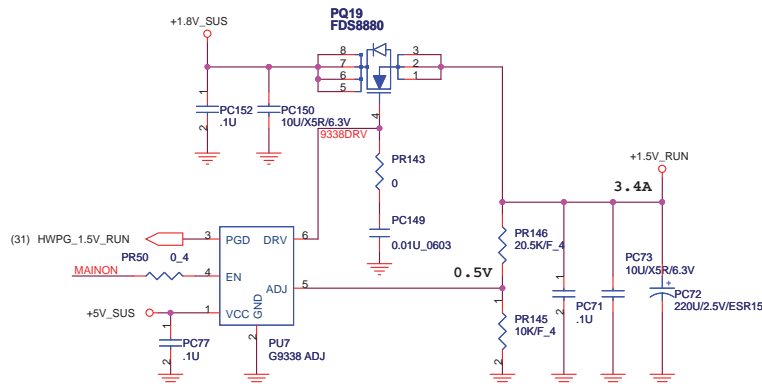
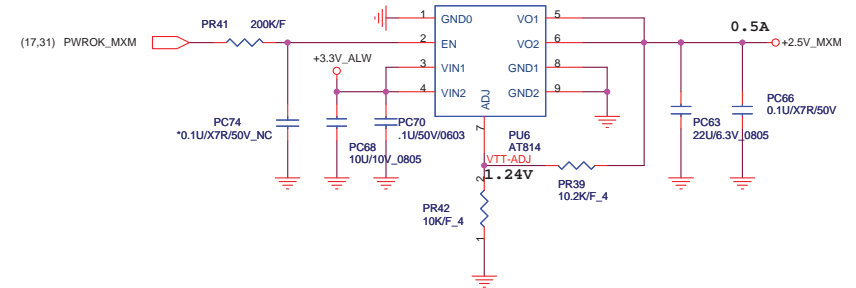
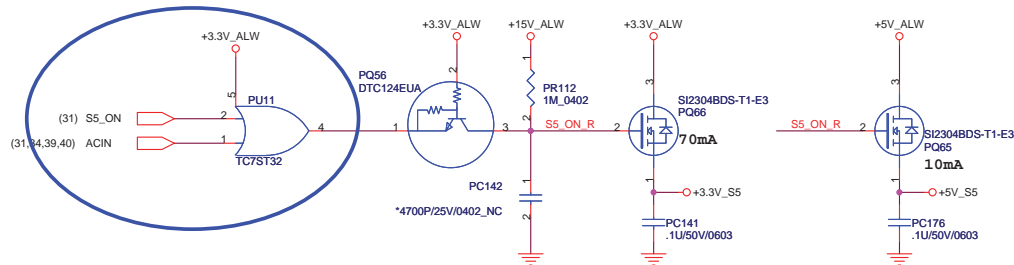
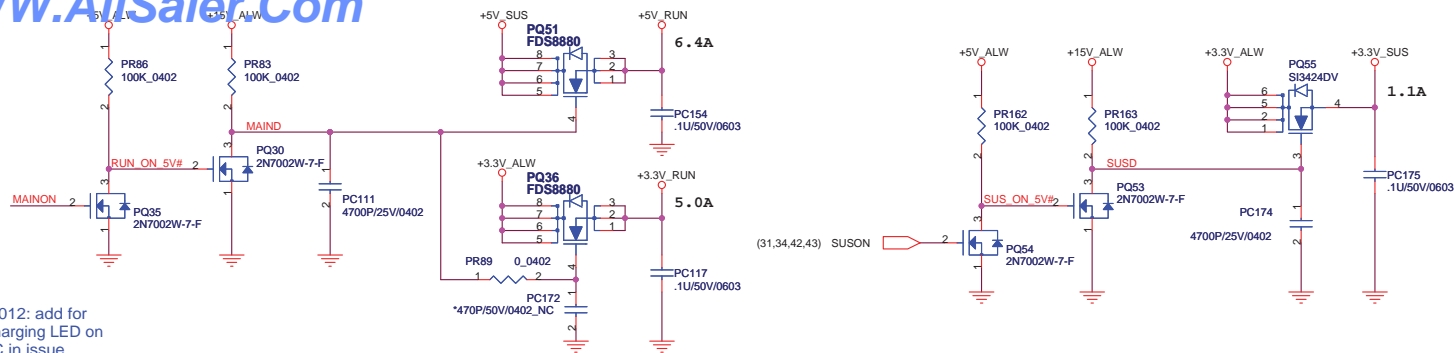
Size: Document Number MX3 Rev 3A

Date: Friday, October 12, 2007 Sheet 40 of 53



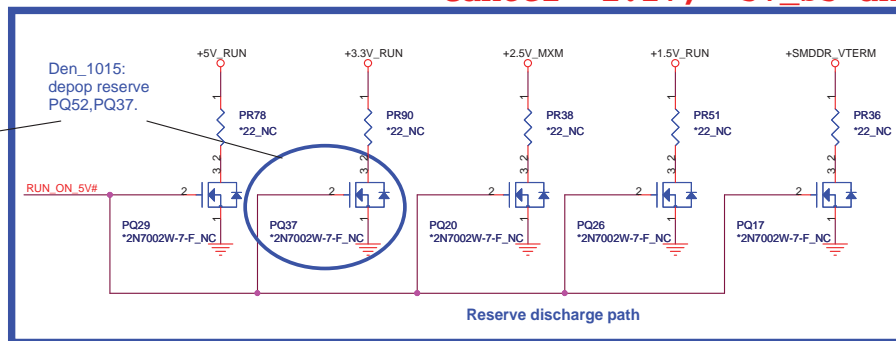
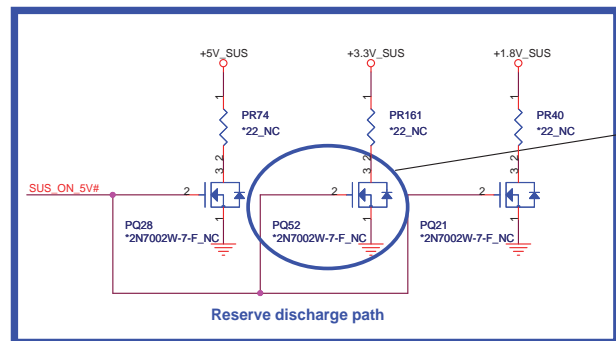


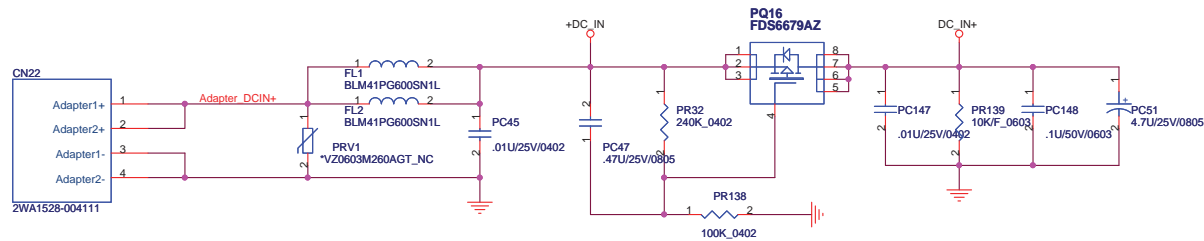
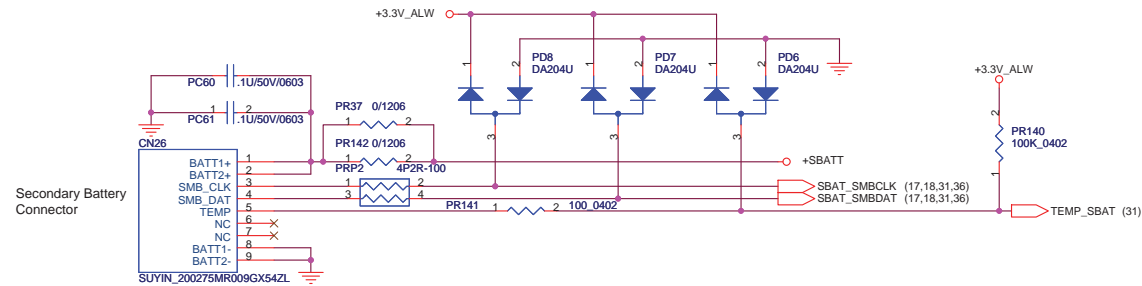
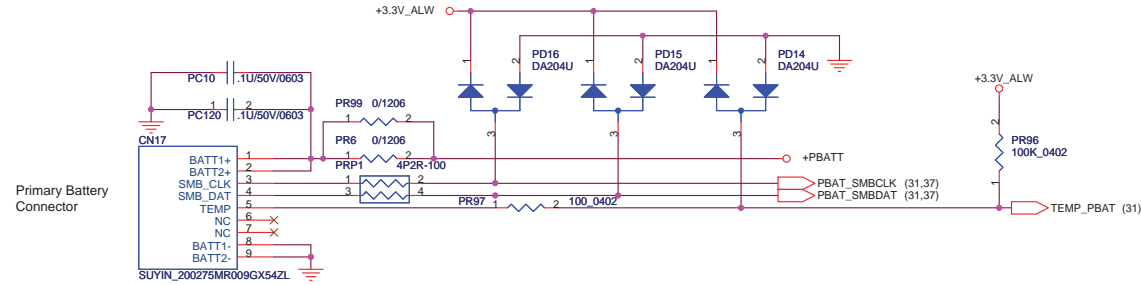




Cancel +1.2V, +5V_S5 and +1.5V_S5

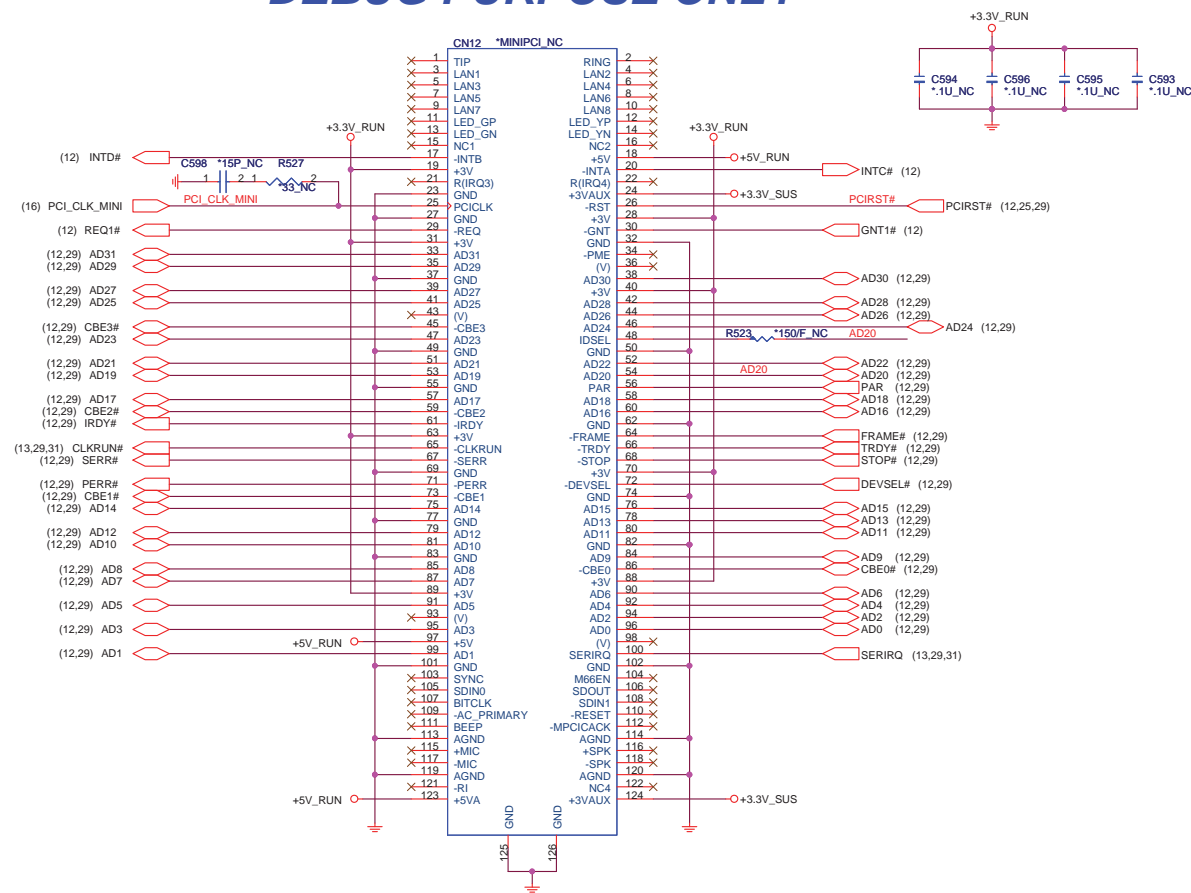
PR33= 32.4K for +1.25_RUN rising up to 1.28V

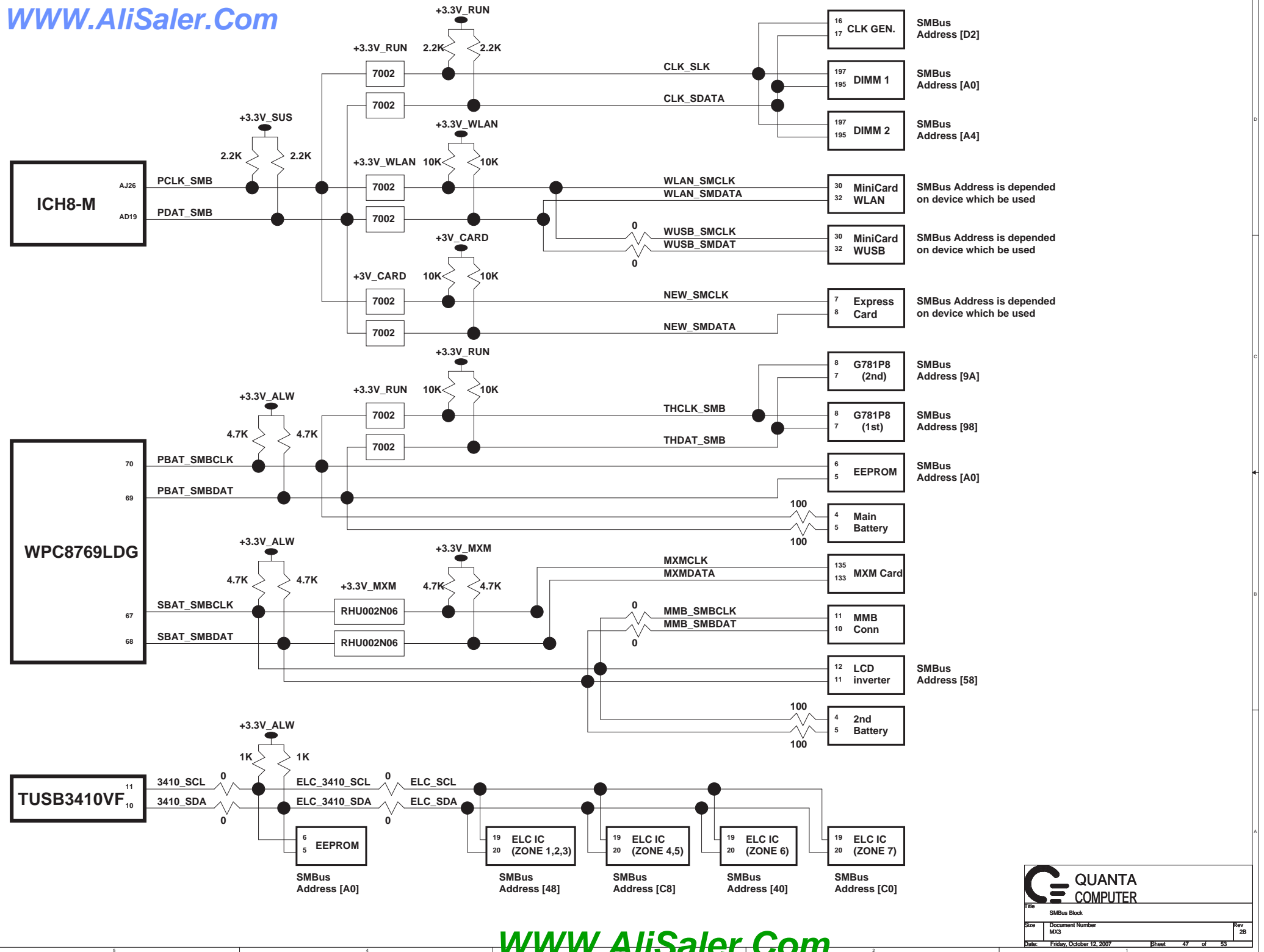


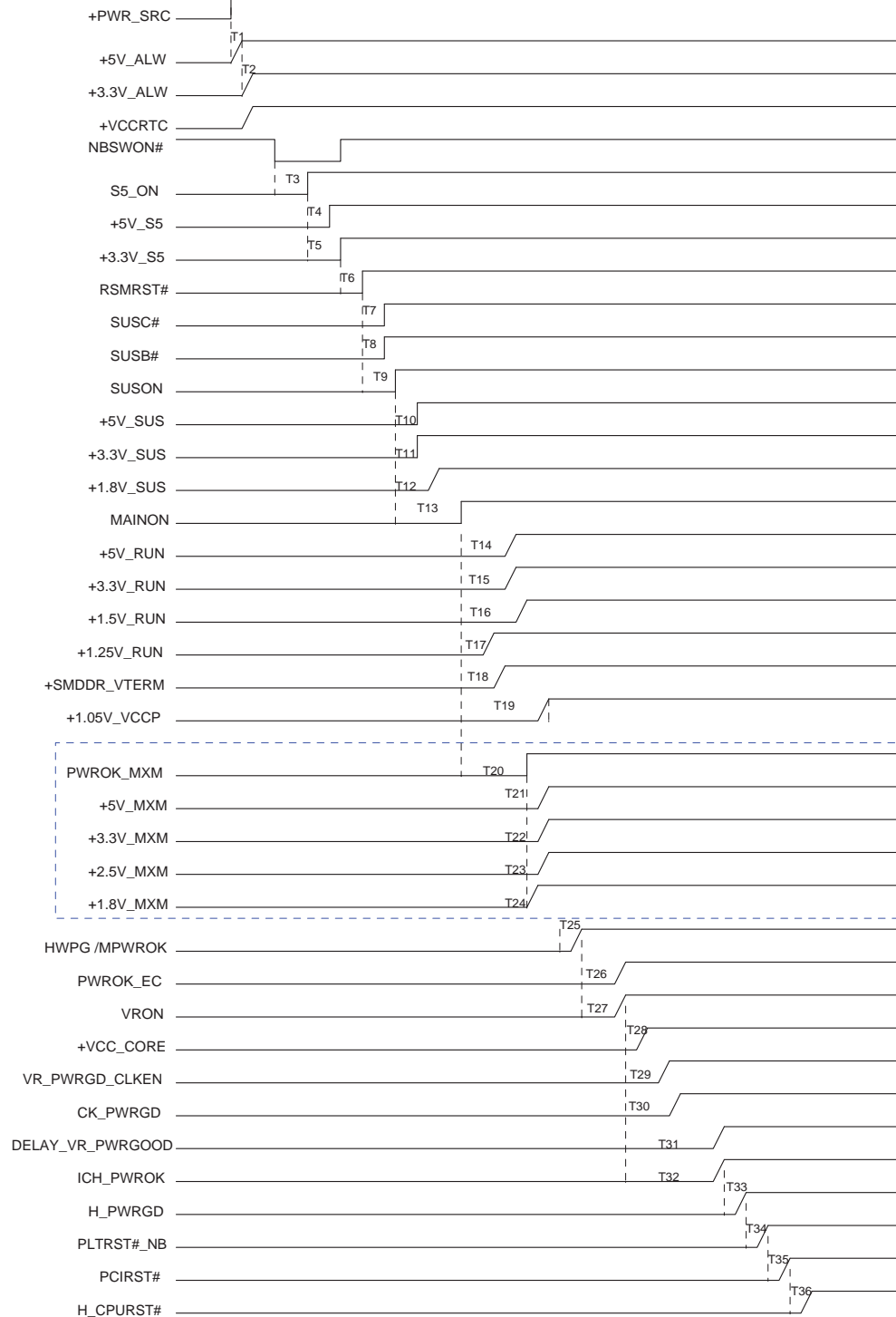


Interrupt Pin : INTC#, INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#

DEBUG PURPOSE ONLY







For MXM
Card Power

MX3 Power On Timing

ITEM	Measure Point		Time
T1	+PWR_SRC	To +5V_ALW	
T2	+5V_ALW	To +3.3V_ALW	
T3	NBSWON#	To S5_ON	
T4	S5_ON	To +5V_S5	
T5	S5_ON	To +3.3V_S5	
T6	+3.3V_S5	To RSMRST#	
T7	RSMRST#	To SUSC#	
T8	RSMRST#	To SUSB#	
T9	RSMRST#	To SUSON	
T10	SUSON	To +5V_SUS	
T11	SUSON	To +3.3V_SUS	
T12	SUSON	To +1.8V_SUS	
T13	SUSON	To MAINON	
T14	MAINON	To +5V_RUN	
T15	MAINON	To +3.3V_RUN	
T16	MAINON	To +1.5V_RUN	
T17	MAINON	To +1.25V_RUN	
T18	MAINON	To +SMDDR_VTERM	
T19	MAINON	To +1.05V_VCCP	
T20	MAINON	To PWROK_MXM	
T21	PWROK_MXM	To +5V_MXM	
T22	PWROK_MXM	To +3.3V_MXM	
T23	PWROK_MXM	To +2.5V_MXM	
T24	PWROK_MXM	To +1.8V_MXM	
T25	+1.05V_VCCP	To HWPG /MPWROK	
T26	HWPG /MPWROK	To PWROK_EC	
T27	HWPG /MPWROK	To VRON	
T28	VRON	To +VCC_CORE	
T29	VRON	To VR_PWRGD_CLKEN	
T30	VRON	To CK_PWRGD	
T31	VRON	To DELAY_VR_PWRGOOD	
T32	VRON	To ICH_PWROK	
T33	ICH_PWROK	To H_PWRGD	
T34	H_PWRGD	To PLTRST#_NB	
T35	PLTRST#_NB	To PCIRST#	
T36	PCIRST#	To H_CPURST#	

